Applications Note: SY5011

Single Stage Flyback And PFC Controller With CV/CC Control For Adapters and Chargers

General Description

SY5011 is a single stage Flyback and PFC controller with several features to enhance performance of Flyback converters. Both current and voltage regulation are achieved by primary side control technology for low cost application. To achieve higher efficiency and better EMI performance, SY5011 drives Flyback converters in the Quasi-Resonant mode.

Ordering Information

SY5011 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY5011FAC	SO8	----

Features

- Primary side CV/CC control eliminates the opto-coupler.
- Valley turn-on of the primary MOSFET to achieve low switching losses
- Internal high current MOSFET driver: 1A sourcing and 2A sinking
- Power factor >0.90 with single-stage conversion
- Low start up current: 15µA typical
- Maximum switching frequency limitation 200kHz
- Compact package: SO8

Applications

- AC/DC adapters
- Battery Chargers

Typical Applications

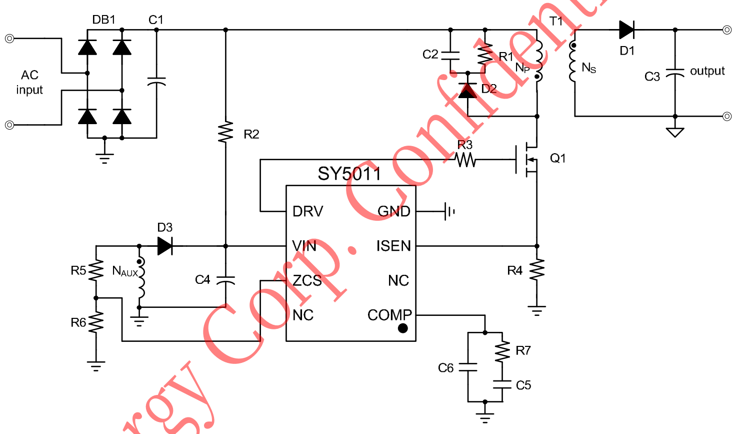


Figure 1. Schematic Diagram

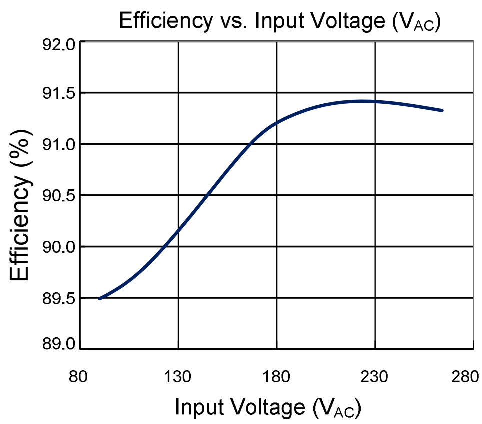
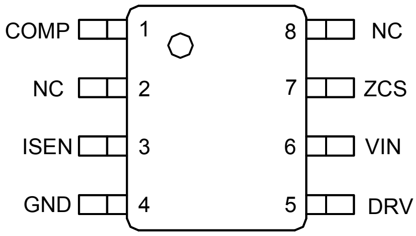


Figure 2. Efficiency vs Input Voltage

Pinout (top view)



(SO8)

Top Mark: AJE*xyz* for SY5011FAC(device code: AJE, ***x=year code, y=week code, z= lot number code***)

Pin	Name	Description
1	COMP	Loop compensation pin. Connect a RC network across this pin and ground to stabilize the control loop.
3	ISEN	Current sense pin. Connect this pin to the source of the primary switch.
4	GND	Ground pin.
5	DRV	Gate driver pin. Connect this pin to the gate of primary MOSFET.
6	VIN	Power supply pin.
7	ZCS	Inductor current zero-crossing detection pin. This pin receives the auxiliary winding voltage by a resistor divider and detects the inductor current zero crossing point.

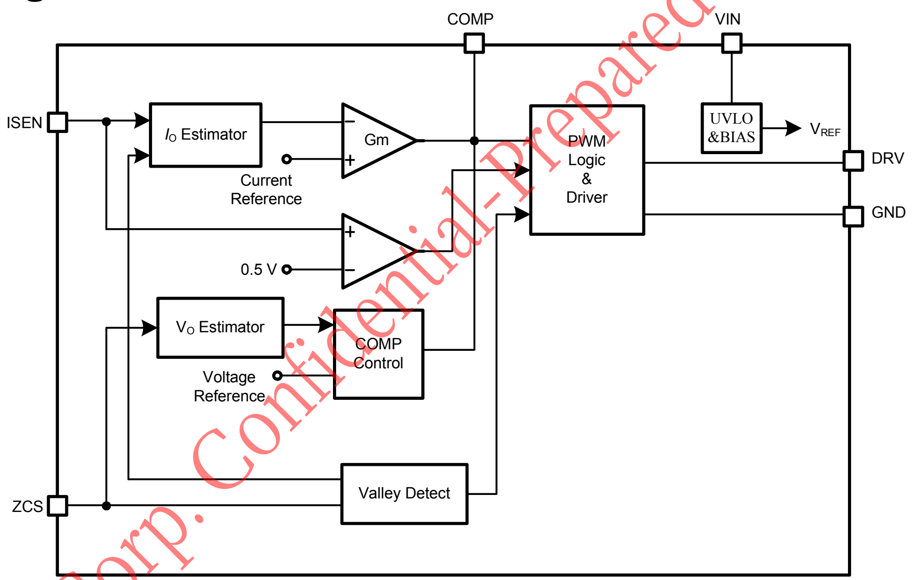
Absolute Maximum Ratings (Note 1)

VIN, DRV -- -0.3V to 19V
Supply current I_{VIN} -- 30mA
ZCS -- -0.3V to V_{IN}+0.3V
ISEN, COMP -- -0.3V~3.6V
Power Dissipation, @ T_A = 25°C SO8 -- 1.1W
Package Thermal Resistance (Note 2)
SO8, θ_{JA} -- 88°C/W
SO8, θ_{JC} -- 45°C/W
Temperature Range -- -40°C to 150°C
Lead Temperature (Soldering, 10 sec.) -- 260°C
Storage Temperature Range -- -65°C to 150°C

Recommended Operating Conditions (Note 3)

VIN, DRV -- 8V~15.4V
Junction Temperature Range -- -40°C to 125°C
Ambient Temperature Range -- -40°C to 85°C

Block Diagram



Electrical Characteristics

(V_{IN} = 12V (Note 3), T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply Section						
Input voltage range	V_{VIN}		8		15.4	V
VIN turn-on threshold	$V_{VIN,ON}$				17.6	V
VIN turn-off threshold	$V_{VIN,OFF}$		6.0		7.9	V
VIN OVP voltage	$V_{VIN,OVP}$			$V_{VIN,ON}$+0.85		V
Start up Current	I_{ST}	V_{VIN}<$V_{VIN,OFF}$		15		µA
Operating Current	I_{VIN}	C_L=100pF,f=15kHz		1		mA
Shunt current in OVP mode	$I_{VIN,OVP}$	V_{VIN}>$V_{VIN,OVP}$	1.6	2	2.5	mA
Error Amplifier Section						
Sleep mode ON threshold on COMP	$V_{COMP,ON}$			0.40		V
Sleep mode OFF threshold on COMP	$V_{COMP,OFF}$			0.48		V
Current Sense Section						
Current limit reference voltage	$V_{ISEN,MAX}$			0.5		V
ZCS pin Section						
ZCS pin OVP voltage threshold	$V_{ZCS,OVP}$			$V_{ZCS,REF}$×(1+6%)		V
ZCS pin voltage reference	$V_{ZCS,REF}$		1.225	1.25	1.275	V
Gate Driver Section						
Gate driver voltage	V_{Gate}			V_{VIN}		V
Maximum source current	I_{SOURCE}			1		A
Minimum sink current	I_{SINK}			2		A
Max ON Time	$T_{ON,MAX}$	V_{COMP}=1.5V		24		µs
Min ON Time	$T_{ON,MIN}$			400		ns
Max OFF Time	$T_{OFF,MAX}$			39		µs
Min OFF Time	$T_{OFF,MIN}$			1		µs
Maximum switching frequency	f_{MAX}			125		kHz
Thermal Section						
Thermal Shutdown Temperature	T_{SD}			150		℃

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on 2" x 2" FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.

Note 3: Increase VIN pin voltage gradually higher than $V_{VIN,ON}$ voltage then turn down to 12V.

Operation

SY5011 is a constant current Flyback controller with primary side control and PFC function that targets at LED lighting applications.

The Device provides primary side control to eliminate the opto-couplers or the secondary feedback circuits, which would cut down the cost of the system.

High power factor is achieved by constant on operation mode, with which the control scheme and the circuit structure are both simple.

In order to reduce the switching losses and improve EMI performance, Quasi-Resonant switching mode is applied, which means to turn on the power MOSFET at voltage valley; the start up current of SY011 is rather small (15μA typically) to reduce the standby power loss further.

SY5011 provides reliable protections such as Over Voltage Protection (VOP), Short Circuit Protection (SCP), Over Temperature Protection (OTP), etc.

SY5011 is available with SO8 package.

Applications Information

Start up

After AC supply or DC BUS is powered on, the capacitor C_{VIN} across VIN and GND pin is charged up by BUS voltage through a start up resistor R_{ST}. Once V_{VIN} rises up to $V_{VIN\text{-}ON}$, the internal blocks start to work. V_{VIN} will be pulled down by internal consumption of IC until the auxiliary winding of Flyback transformer could supply enough energy to maintain V_{VIN} above $V_{VIN\text{-}OFF}$.

The whole start up procedure is divided into two sections shown in Fig.3. t_{STC} is the C_{VIN} charged up section, and t_{STO} is the output voltage built-up section. The start up time t_{ST} composes of t_{STC} and t_{STO}, and usually t_{STO} is much smaller than t_{STC}.

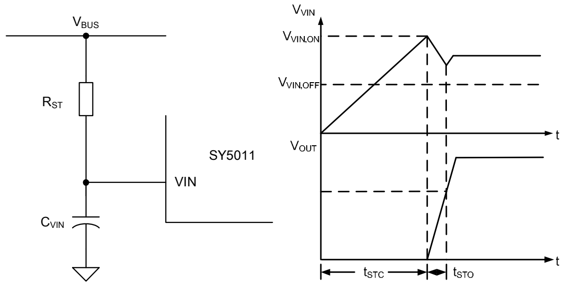


Fig.3 Start up

The start up resistor R_{ST} and C_{VIN} are designed by rules below:

(a) Preset start-up resistor R_{ST}, make sure that the current through R_{ST} is larger than I_{ST} and smaller than I_{VIN_OVP}

$$\frac{V_{BUS}}{I_{VIN\_OVP}} < R_{ST} < \frac{V_{BUS}}{I_{ST}} \quad (1)$$

Where V_{BUS} is the BUS line voltage.

(b) Select C_{VIN} to obtain an ideal start up time t_{ST}, and ensure the output voltage is built up at one time.

$$C_{VIN} = \frac{(\frac{V_{BUS}}{R_{ST}} - I_{ST}) \times t_{ST}}{V_{VIN\_ON}} \quad (2)$$

(c) If the C_{VIN} is not big enough to build up the output voltage at one time. Increase C_{VIN} and decrease R_{ST}, go back to step (a) and redo such design flow until the ideal start up procedure is obtained.

Shut down

After AC supply or DC BUS is powered off, the energy stored in the BUS capacitor will be discharged. When the auxiliary winding of Flyback transformer can not supply enough energy to VIN pin, V_{VIN} will drop down. Once V_{VIN} is below $V_{VIN\text{-}OFF}$, the IC will stop working and V_{COMP} will be discharged to zero.

Quasi-Resonant Operation

QR mode operation provides low turn-on switching losses for Flyback converter.

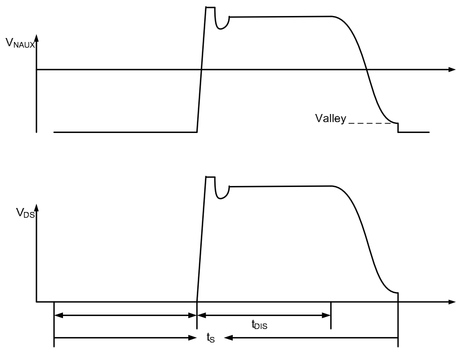


Fig.4 QR mode operation

The voltage across drain and source of the primary MOSFET is reflected by the auxiliary winding of the Flyback transformer. ZCS pin detects the voltage across the auxiliary winding by a resistor divider. When the voltage across drain and source of the primary MOSFET is at voltage valley, the MOSFET would be turned on.

Output Voltage Control

In order to achieve primary side constant voltage control, the output voltage is detected by the auxiliary winding voltage.

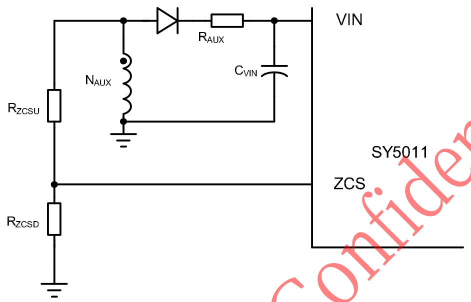


Fig.5 ZCS pin connection

As shown in Fig.6, during OFF time, the voltage across the auxiliary winding is

$$V_{AUX} = (V_{OUT} + V_{D,F}) \times \frac{N_{AUX}}{N_S} \quad (3)$$

N_{AUX} is the turns of auxiliary winding; N_S is the turns of secondary winding; $V_{D,F}$ is the forward voltage of the power diode.

At the current zero-crossing point, $V_{D,F}$ is nearly zero, so V_{OUT} is proportional with V_{AUX} exactly. The voltage of this point is sampled by the IC as the feedback of output voltage. The resistor divider is designed by

$$\frac{V_{ZCS,REF}}{V_{OUT}} = \frac{R_{ZCSD}}{R_{ZCSU} + R_{ZCSD}} \times \frac{N_{AUX}}{N_S} \quad (4)$$

Where $V_{ZCS,REF}$ is the internal voltage reference.

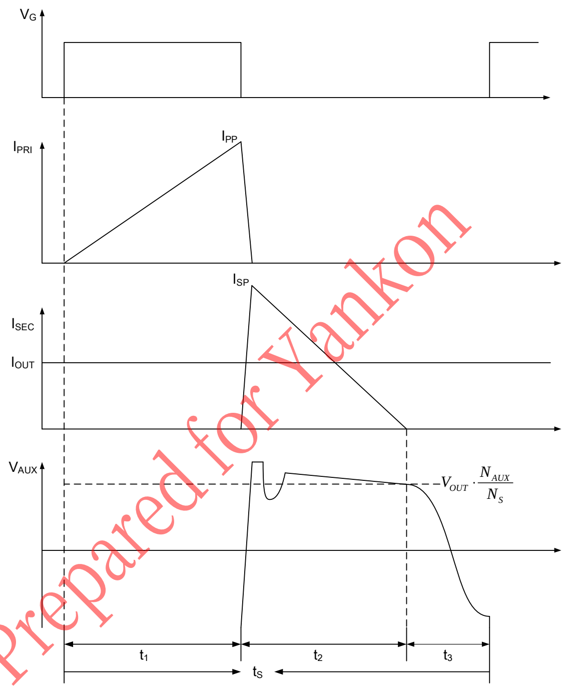


Fig.6 Auxiliary winding voltage waveforms

Output Current Control

The output current is regulated by SY5011 with primary side detection technology, the maximum output current $I_{OUT,LIM}$ can be set by

$$I_{OUT,LIM} = \frac{k_1 \times k_2 \times V_{REF} \times N_{PS}}{R_S} \quad (5)$$

Where k_1 is the output current weight coefficient; k_2 is the output modification coefficient; V_{REF} is the internal reference voltage; R_S is the current sense resistor.

k_1, k_2 and V_{REF} are all internal constant parameters, $I_{OUT,LIM}$ can be programmed by N_{PS} and R_S.

$$R_S = \frac{k_1 \times k_2 \times V_{REF} \times N_{PS}}{I_{OUT}} \quad (6)$$

When over current operation or short circuit operation happens, the output current will be limited at $I_{OUT,LIM}$. The V-I curve is shown as Fig.7.

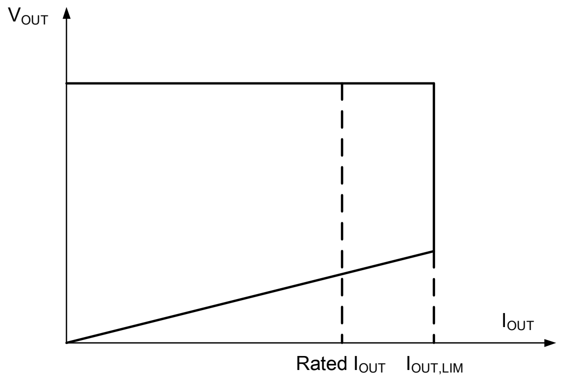


Fig.7 V-I curve

The IC provides line regulation modification function to improve line regulation performance of the output current.

Due to the sample delay of ISEN pin and other internal delay, the output current increases with increasing input BUS line voltage. A small compensation voltage ΔV_{ISEN-C} is added to ISEN pin during ON time to improve such performance. This ΔV_{ISEN-C} is adjusted by the upper resistor of the divider connected to ZCS pin.

$$\Delta V_{ISEN,C} = V_{BUS} \times \frac{N_{AUX}}{N_P} \times \frac{1}{R_{ZCSU}} \times k_3 \quad (7)$$

Where R_{ZCSU} is the upper resistor of the divider; k3 is an internal constant as the modification coefficient.

The compensation is mainly related with R_{ZCSU}, larger compensation is achieved with smaller R_{ZCSU}. Normally, R_{ZCS} ranges from 100kΩ~1MΩ.

Short Circuit Protection (SCP)

When the output is shorted to ground, the output voltage is clamped to zero. The voltage of the auxiliary winding is proportional to the output winding, so V_{VIN} will drop down without auxiliary winding supply. Once V_{VIN} is below $V_{VIN,OFF}$, the IC will shut down and be charged again by the BUS voltage through the start up resistor. If the short circuit condition still exists, the system will operate in hiccup mode.

Power Device Design

MOSFET and Diode

When the operation condition is with maximum input voltage and full load, the voltage stress of MOSFET and secondary power diode is maximized;

$$V_{MOS\_DS\_MAX} = \sqrt{2} V_{AC\_MAX} + N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S \quad (8)$$

$$V_{D\_R\_MAX} = \frac{\sqrt{2} V_{AC\_MAX}}{N_{PS}} + V_{OUT} \quad (9)$$

Where $V_{AC,MAX}$ is maximum input AC RMS voltage; N_{PS} is the turns ratio of the Flyback transformer; V_{OUT} is the rated output voltage; $V_{D,F}$ is the forward voltage of secondary power diode; ΔV_S is the overshoot voltage clamped by RCD snubber during OFF time.

When the operation condition is with minimum input voltage and full load, the current stress of MOSFET and power diode is maximized.

$$I_{MOS\_PK\_MAX} = I_{P\_PK\_MAX} \quad (10)$$

$$I_{MOS\_RMS\_MAX} = I_{P\_RMS\_MAX} \quad (11)$$

$$I_{D\_PK\_MAX} = N_{PS} \times I_{P\_PK\_MAX} \quad (12)$$

$$I_{D\_AVG} = I_{OUT} \quad (13)$$

Where $I_{P-PK-MAX}$ and $I_{P-RMS-MAX}$ are maximum primary peak current and RMS current, which will be introduced later.

Transformer (N_{PS} and L_M)

N_{PS} is limited by the electrical stress of the power MOSFET:

$$N_{PS} \le \frac{V_{MOS\_(BR)DS} \times 90\% - \sqrt{2} V_{AC\_MAX} - \Delta V_S}{V_{OUT} + V_{D\_F}} \quad (14)$$

Where $V_{MOS,(BR)DS}$ is the breakdown voltage of the power MOSFET.

In Quasi-Resonant mode, each switching period cycle t_S consists of three parts: current rising time t_1, current falling time t_2 and quasi-resonant time t_3 shown in

Fig.8.

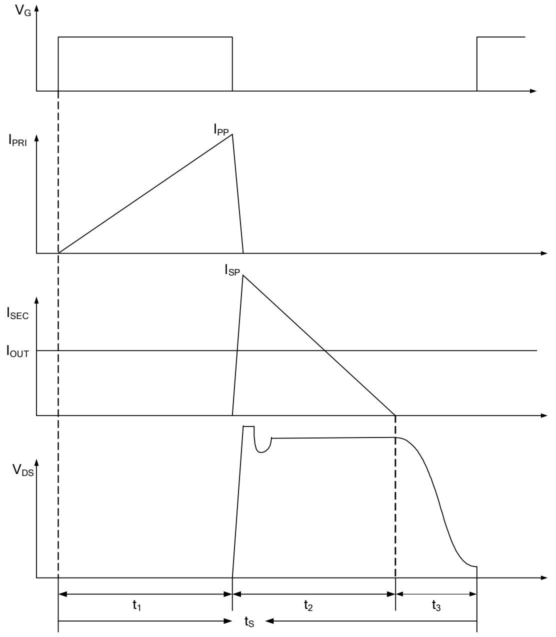


Fig.8 switching waveforms

The system operates in the constant on time mode to achieve high power factor. The ON time increases with the input AC RMS voltage decreasing and the load increasing. When the operation condition is with minimum input AC RMS voltage and full load, the ON time is maximized. On the other hand, when the input voltage is at the peak value, the OFF time is maximized. Thus, the minimum switching frequency $f_{S\text{-}MIN}$ happens at the peak value of input voltage with minimum input AC RMS voltage and maximum load condition; meanwhile, the maximum peak current through MOSFET and the transformer happens.

Once the minimum frequency $f_{S\text{-}MIN}$ is set, the inductance of the transformer could be induced. The design flow is shown as below:

(a) Select N_{PS}

$$N_{PS} \le \frac{V_{MOS\_(BR)DS} \times 90\% - \sqrt{2}V_{AC\_MAX} - \Delta V_S}{V_{OUT} + V_{D\_F}} \quad (15)$$

(b) Preset minimum frequency $f_{S\text{-}MIN}$

(c) Compute relative t_S, t_1 (t_3 is omitted to simplify the design here)

$$t_S = \frac{1}{f_{S\_MIN}} \quad (16)$$

$$t_1 = \frac{t_S \times N_{PS} \times (V_{OUT} + V_{D\_F})}{\sqrt{2}V_{AC\_MIN} + N_{PS} \times (V_{OUT} + V_{D\_F})} \quad (17)$$

(d) Design inductance L_M

$$L_M = \frac{V_{AC\_MIN}^2 \times t_1^2 \times \eta}{2P_{OUT} \times t_S} \quad (18)$$

(e) Compute t_3

$$t_3 = \pi \times \sqrt{L_M \times C_{Drain}} \quad (19)$$

Where C_{Drain} is the parasitic capacitance at drain of MOSFET.

(f) Compute primary maximum peak current $I_{P\text{-}PK\text{-}MAX}$ and RMS current $I_{P\text{-}RMS\text{-}MAX}$ for the transformer fabrication.

$$I_{P\_PK\_MAX} = \frac{2P_{OUT} \times [\frac{L_M}{\sqrt{2}V_{AC\_MIN}} + \frac{L_M}{N_{PS} \times (V_{OUT} + V_{D\_F})}]}{L_M \times \eta} + \frac{\sqrt{4P_{OUT}^2 \times [\frac{L_M}{\sqrt{2}V_{AC\_MIN}} + \frac{L_M}{N_{PS} \times (V_{OUT} + V_{D\_F})}]^2 + 4L_M \times \eta \times P_{OUT} \times t_3}}{L_M \times \eta}$$

(20)

Where η is the efficiency; P_{OUT} is rated full load power

Adjust t_1 and t_S to t_1' and t_S' considering the effect of t_3

$$t_S' = \frac{\eta \times L_M \times I_{P\_PK\_MAX}^2}{4P_{OUT}} \quad (21)$$

$$t_1' = \frac{L_M \times I_{P\_PK\_MAX}}{\sqrt{2}V_{AC\_MIN}} \quad (22)$$

$$I_{P\_RMS\_MAX} \approx \sqrt{\frac{t_1'}{6t_S'}} \times I_{P\_PK\_MAX} \quad (23)$$

(g) Compute secondary maximum peak current $I_{S\text{-}PK\text{-}MAX}$ and RMS current $I_{S\text{-}RMS\text{-}MAX}$ for the transformer fabrication.

$$I_{S\_PK\_MAX} = N_{PS} \times I_{P\_PK\_MAX} \quad (24)$$

$$t_2' = t_S' - t_1' - t_3 \quad (25)$$

$$I_{S\_RMS\_MAX} \approx \sqrt{\frac{t_2'}{6t_S'}} \times I_{S\_PK\_MAX} \quad (26)$$

Transformer design (N_P,N_S,N_{AUX})

The design of the transformer is similar with ordinary Flyback transformer. the parameters below are necessary:

Necessary parameters	
Turns ratio	N_{PS}
Inductance	L_M
Primary maximum current	$I_{P\text{-}PK\text{-}MAX}$
Primary maximum RMS current	$I_{P\text{-}RMS\text{-}MAX}$
Secondary maximum RMS current	$I_{S\text{-}RMS\text{-}MAX}$

The design rules are as followed:

(a) Select the magnetic core style, identify the effective area A_e.

(b) Preset the maximum magnetic flux ΔB

ΔB=0.22~0.26T

(c) Compute primary turn N_P

$$N_P = \frac{L_M \times I_{P\_PK\_MAX}}{\Delta B \times A_e} \quad (27)$$

(d) Compute secondary turn N_S

$$N_S = \frac{N_P}{N_{PS}} \quad (28)$$

(e) compute auxiliary turn N_{AUX}

$$N_{AUX} = N_S \times \frac{V_{VIN}}{V_{OUT}} \quad (29)$$

Where V_{VIN} is the working voltage of VIN pin (10V~11V is recommended).

(f) Select an appropriate wire diameter

With $I_{P\text{-}RMS\text{-}MAX}$ and $I_{S\text{-}RMS\text{-}MAX}$, select appropriate wire to make sure the current density ranges from 4A/mm^2 to 10A/mm^2.

(g) If the winding area of the core and bobbin is not enough, reselect the core style, go to **(a)** and redesign the transformer until the ideal transformer is achieved.

Output capacitor C_{OUT}

Preset the output voltage ripple ΔV_{OUT}, C_{OUT} is induced by

$$C_{OUT} = \sqrt{\frac{\left(\frac{2I_{OUT}}{\Delta V_{OUT}/R_{LOAD}}\right)^2 - 1}{4 f_{AC} R_{LOAD} \pi}} \quad (30)$$

Where I_{OUT} is the output current; ΔV_{OUT} is the demanded voltage ripple; f_{AC} is the input AC supply frequency; R_{LOAD} is the load.

RCD snubber for MOSFET

The power loss of the snubber P_{RCD} is evaluated first

$$P_{RCD} = \frac{N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S}{\Delta V_S} \times \frac{L_K}{L_M} \times P_{OUT} \quad (31)$$

Where N_{PS} is the turns ratio of the Flyback transformer; V_{OUT} is the output voltage; $V_{D\text{-}F}$ is the forward voltage of the power diode; ΔV_S is the overshoot voltage clamped by RCD snubber; L_K is the leakage inductor; L_M is the inductance of the Flyback transformer; P_{OUT} is the output power.

The R_{RCD} is related with the power loss:

$$R_{RCD} = \frac{(N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S)^2}{P_{RCD}} \quad (32)$$

The C_{RCD} is related with the voltage ripple of the snubber $\Delta V_{C\text{-}RCD}$:

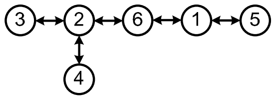
$$C_{RCD} = \frac{N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S}{R_{RCD} f_S \Delta V_{C\_RCD}} \quad (33)$$

Layout

(a) To achieve better EMI performance and reduce line frequency ripples, the output of the bridge rectifier should be connected to the BUS line capacitor first, then to the switching circuit.

(b) The circuit loop of all switching circuit should be kept small: primary power loop, secondary loop and auxiliary power loop.

(c) The connection of primary ground is recommended as:



Ground ①: ground of BUS line capacitor
Ground ②: ground of bias supply capacitor
Ground ③: ground node of auxiliary winding
Ground ④: ground of signal trace
Ground ⑤: primary ground node of Y capacitor
Ground ⑥: ground node of current sample resistor.

(d) bias supply trace should be connected to the bias supply capacitor first instead of GND pin. The bias supply capacitor should be put beside the IC.

(e) Loop of ‘Source pin – current sample resistor – GND pin’ should be kept as small as possible.

(f) The resistor divider connected to ZCS pin is recommended to be put beside the IC.

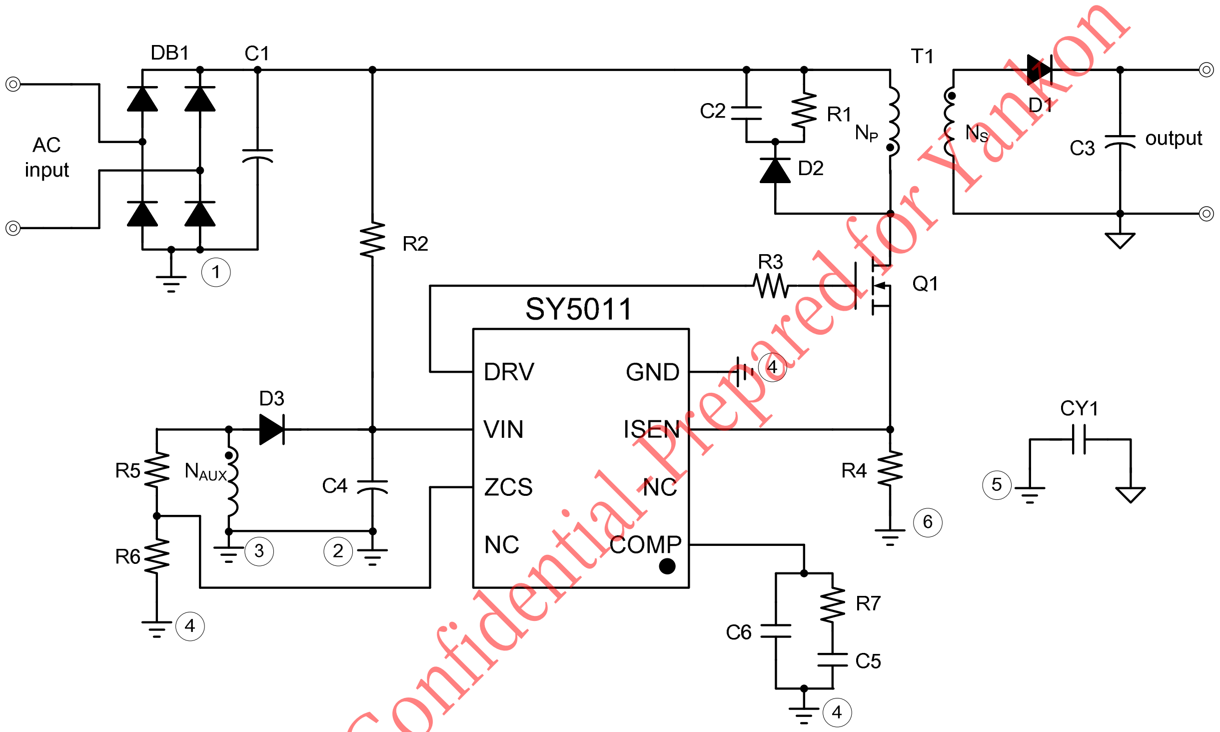


Fig.9.GND connection recommended

Design Example

A design example of typical application is shown below step by step.

#1. Identify design specification

Design Specification			
V_{AC}(RMS)	90V~264V	V_{OUT}	53V
I_{OUT}	1.2A	η	90%

#2. Transformer design (N_{PS}, L_M)

Refer to Power Device Design

Conditions			
$V_{AC,MIN}$	90V	V_{AC-MAX}	264V
ΔV_S	100V	$V_{MOS-(BR)DS}$	800V
P_{OUT}	60W	$V_{D,F}$	1V
C_{Drain}	100pF	f_{S-MIN}	50kHz

(a) Compute turns ratio N_{PS} first

$$N_{PS} \le \frac{V_{MOS\_(BR)DS} \times 90\% - \sqrt{2} V_{AC\_MAX} - \Delta V_S}{V_{OUT} + V_{D,F}}$$

$$= \frac{800V \times 0.9 - \sqrt{2} \times 264V - 100V}{53V + 1V}$$

$$= 4.57$$

N_{PS} is set to

$$N_{PS} = 2.05$$

(b)$f_{S,MIN}$ is preset

$$f_{S\_MIN} = 50kHz$$

(c) Compute the switching period t_S and ON time t_1 at the peak of input voltage.

$$t_S = \frac{1}{f_{S\_MIN}} = 20\mu s$$

$$t_1 = \frac{t_S \times N_{PS} \times (V_{OUT} + V_{D\_F})}{\sqrt{2} V_{AC\_MIN} + N_{PS} \times (V_{OUT} + V_{D\_F})}$$

$$= \frac{20\mu s \times 2.05 \times (53V + 1V)}{\sqrt{2} \times 90V + 2.05 \times (53V + 1V)}$$

$$= 9.3\mu s$$

(d) Compute the inductance L_M

$$L_M = \frac{V_{AC\_MIN}^2 \times t_1^2 \times \eta}{2P_{OUT} \times t_S}$$
$$= \frac{(\sqrt{2} \times 90V)^2 \times 9.3\mu s^2 \times 0.9}{2 \times 60W \times 20\mu s}$$
$$= 523\mu H$$

Set

$$L_M = 280\mu H$$

(e) Compute the quasi-resonant time t_3

$$t_3 = \pi \times \sqrt{L_M \times C_{Drain}}$$
$$= \pi \times \sqrt{280\mu H \times 100pF}$$
$$= 525ns$$

(f) Compute primary maximum peak current $I_{P\text{-}PK\text{-}MAX}$

$$I_{P\_PK\_MAX} = \frac{2P_{OUT} \times [\frac{L_M}{\sqrt{2}V_{AC\_MIN}} + \frac{L_M}{N_{PS} \times (V_{OUT} + V_{D\_F})}]}{L_M \times \eta} + \frac{\sqrt{4P_{OUT}^2 \times [\frac{L_M}{\sqrt{2}V_{AC\_MIN}} + \frac{L_M}{N_{PS} \times (V_{OUT} + V_{D\_F})}]^2 + 4L_M \times \eta \times P_{OUT} \times t_3}}{L_M \times \eta}$$
$$= 4.87A$$

Adjust switching period t_S and ON time t_1 to t_S' and t_1'.

$$t_S' = \frac{\eta \times L_M \times I_{P\_PK\_MAX}^2}{4P_{OUT}}$$
$$= \frac{0.9 \times 280\mu H \times 4.87A^2}{4 \times 60W}$$
$$= 23.5\mu s$$

$$t_1' = \frac{L_M \times I_{P\_PK\_MAX}}{\sqrt{2}V_{AC\_MIN}}$$
$$= \frac{280\mu H \times 4.87A}{\sqrt{2} \times 90V}$$
$$= 10.74\mu s$$

Compute primary maximum RMS current $I_{P\text{-}RMS\text{-}MAX}$

$$I_{P\_RMS\_MAX} \approx \sqrt{\frac{t_1'}{6t_S'}} \times I_{P\_PK\_MAX} = \sqrt{\frac{10.74\mu s}{6 \times 23.5\mu s}} \times 4.87A = 1.34A$$

(g) Compute secondary maximum peak current and the maximum RMS current.

$$I_{S\_PK\_MAX}=N_{PS}\times I_{P\_PK\_MAX}=2.05\times 4.87A=9.99A$$

$$t_2^{'}=t_S^{'}-t_1^{'}-t_3=23.5\mu s-10.73\mu s-0.525\mu s=12.25\mu s$$

$$I_{S,RMS,MAX}\approx\sqrt{\frac{t_2^{\prime}}{6t_S^{\prime}}}\times I_{S\_PK\_MAX}=\sqrt{\frac{12.25\mu s}{6\times 23.5\mu s}}\times 9.99A=3.01A$$

#3. Select power MOSFET and secondary power diode

Refer to Power Device Design

Known conditions at this step			
$V_{AC\text{-}MAX}$	264V	N_{PS}	2.05
V_{OUT}	53V	$V_{D\text{-}F}$	1V
ΔV_S	100V	η	90%

(a) Compute the voltage and the current stress of MOSFET:

$$\begin{aligned}V_{MOS\_DS\_MAX}&=\sqrt{2}V_{AC\_MAX}+N_{PS}\times(V_{OUT}+V_{D\_F})+\Delta V_S\\&=\sqrt{2}\times 264V+2.05\times(53V+1V)+100V\\&=585V\end{aligned}$$

$$I_{MOS\_PK\_MAX}=I_{P\_PK\_MAX}=4.87A$$

$$I_{MOS\_RMS\_MAX}=I_{P\_RMS\_MAX}=1.34A$$

(b) Compute the voltage and the current stress of secondary power diode

$$\begin{aligned}V_{D\_R\_MAX}&=\frac{\sqrt{2}V_{AC\_MAX}}{N_{PS}}+V_{OUT}\\&=\frac{\sqrt{2}\times 264V}{2.05}+53V\\&=235V\end{aligned}$$

$$I_{D\_PK\_MAX}=N_{PS}\times I_{P\_PK\_MAX}=2.05\times 4.87A=9.99A$$

$$I_{D\_AVG}=I_{OUT}=1.2A$$

#4. Select the output capacitor C_{OUT}

Refer to Power Device Design

Conditions			
I_{OUT}	1.2A	ΔV_{OUT}	$0.05V_{OUT}$
f_{AC}	50Hz	R_{LOAD}	44 Ω

The output capacitor is

$$C_{OUT}=\frac{\sqrt{(\frac{2I_{OUT}}{\Delta I_{OUT}})^2\text{-}1}}{4\pi f_{AC}R_{LED}}$$
$$=\frac{\sqrt{(\frac{2\times 1.2A}{0.05\times 1.2A})^2\text{-}1}}{4\pi\times 50Hz\times 44\Omega}$$
$$=1450\mu F$$

#5. Design RCD snubber

Refer to Power Device Design

Conditions			
V_{OUT}	53V	ΔV_S	100V
N_{PS}	2.05	L_K/L_M	0.05%
P_{OUT}	60W		

The power loss of the snubber is

$$P_{RCD}=\frac{N_{PS}\times(V_{OUT}+V_{D\_F})+\Delta V_S}{\Delta V_S}\times\frac{L_K}{L_M}\times P_{OUT}$$
$$=\frac{2.05\times(53V+1V)+100V}{100V}\times 0.005\times 60W$$
$$=0.63W$$

The resistor of the snubber is

$$R_{RCD}=\frac{(N_{PS}\times(V_{OUT}+V_{D\_F})+\Delta V_S)^2}{P_{RCD}}$$
$$=\frac{(2.05\times(53V+1V)+50V)^2}{0.63W}$$
$$=54k\Omega$$

The capacitor of the snubber is

$$C_{RCD}=\frac{N_{PS}\times(V_{OUT}+V_{D\_F})+\Delta V_S}{R_{RCD}f_S\Delta V_{C\_RCD}}$$
$$=\frac{2.05\times(53V+1V)+100V}{54k\Omega\times 100kHz\times 25V}$$
$$=1.5nF$$

#6. Set VIN pin

Refer to Start up

Conditions			
$V_{BUS-MIN}$	90V×1.414	$V_{BUS-MAX}$	264V×1.414
I_{ST}	15μA (typical)	V_{IN-ON}	16V (typical)
$I_{VIN-OVP}$	2mA (typical)	t_{ST}	500ms (designed by user)

(a) R_{ST} is preset

$$R_{ST} < \frac{V_{BUS}}{I_{ST}} = \frac{90V\times1.414}{15\mu A} = 8.48M\Omega\ ,$$

$$R_{ST} > \frac{V_{BUS}}{I_{VIN\_OVP}} = \frac{264V\times1.414}{2mA} = 186k\Omega$$

Set R_{ST}

$$R_{ST} = 250k\Omega\times2 = 500k\Omega$$

(b) Design C_{VIN}

$$C_{VIN} = \frac{(\frac{V_{BUS}}{R_{ST}} - I_{ST})\times t_{ST}}{V_{VIN\_ON}}$$

$$= \frac{(\frac{90V\times1.414}{500k\Omega} - 15\mu A)\times500ms}{16V}$$

$$= 7.5\mu F$$

Set C_{VIN}

$$C_{VIN} = 100\mu F$$

#7 Set COMP pin

Refer to **<u>Internal pre-charge design for quick start up</u>**

Parameters designed			
R_{COMP}	100Ω	$V_{COMP,IC}$	450mV
C_{COMP1}	2μF		

#8 Set current sense resistor to achieve ideal output current

Refer to **Primary-side constant-current control**

Known conditions at this step			
k	0.167	N_{PS}	2.05
V_{REF}	0.3V	I_{OUT}	1.2A

The current sense resistor is
Set OCP_limit 1.4A

$$R_S = \frac{k \times V_{REF} \times N_{PS}}{I_{OUT}}$$

$$= \frac{0.167 \times 0.3V \times 2.05}{1.3A}$$

$$=0.0685\Omega$$

#9 set ZCS pin

Refer to **Line regulation modification** and **Over Voltage Protection (OVP) & Open Loop Protection (OLP)**

First identify R_{ZCSU} need for line regulation.

Known conditions at this step			
k_2	68		
Parameters Designed			
R_{ZCSU}	100kΩ		

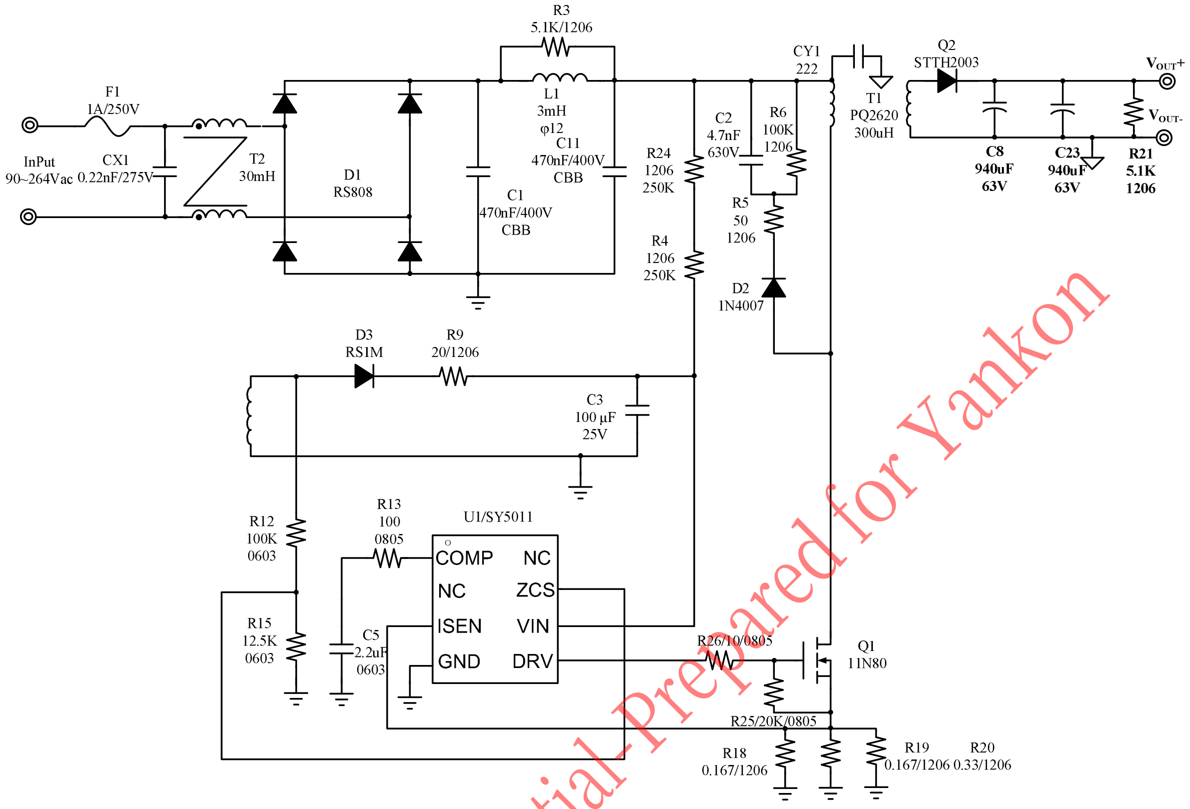
Then compute R_{ZCSD}

Conditions			
V_{OUT}	53V	V_{ZCS_REF}	1.25V
R_{ZCSU}	100kΩ	N_S	2.05
N_{AUX}	4	$V_{ZCS,REF}$	1.25

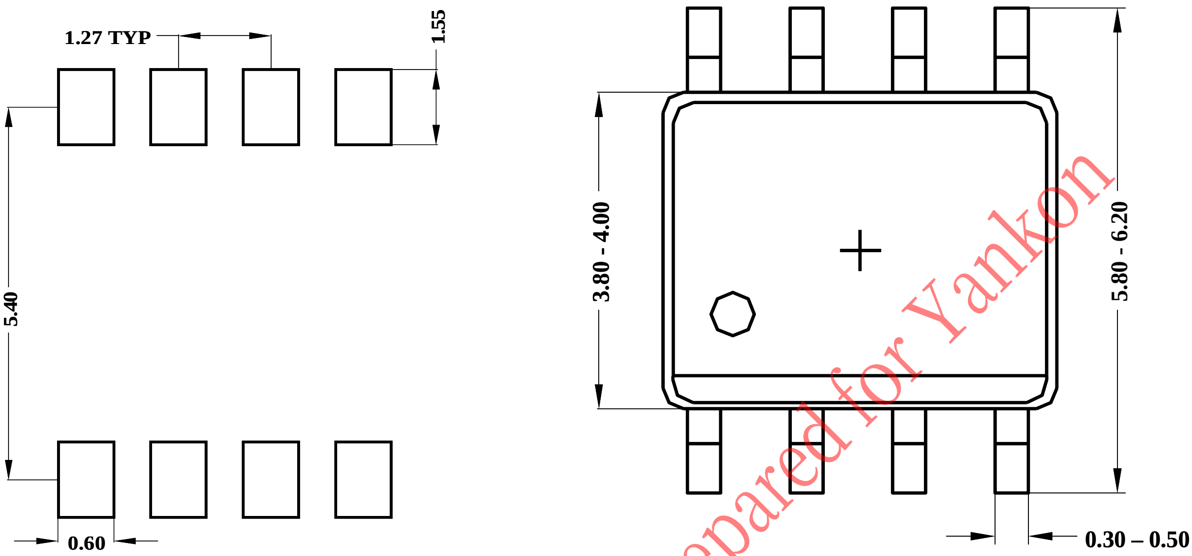
$$R_{ZCSD} = \frac{R_{ZCSU}}{\frac{V_{OUT} N_{AUL}}{V_{ZCS,REF} N_S} - 1} = \frac{100K}{(\frac{53V \times 4}{1.25V \times 20} - 1)} = 13.3K$$

$$R_{ZCSD} = 12.8k\Omega$$

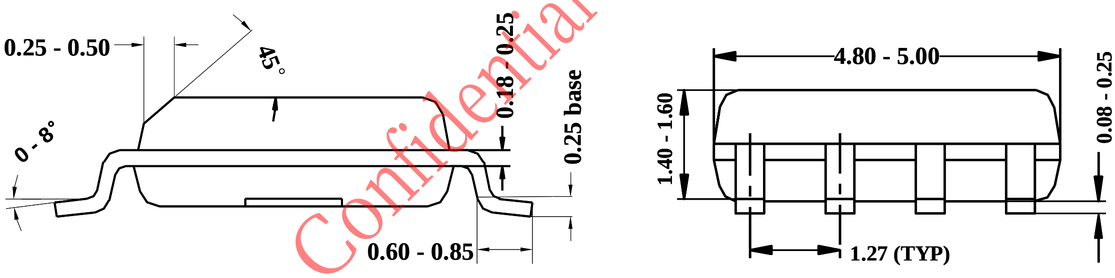
#10 final result



SO8 Package Outline & PCB Layout Design



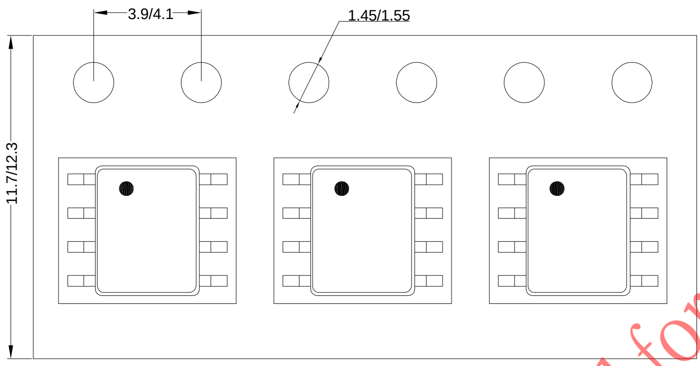
Recommended Pad Layout



Notes: All dimensions are in millimeters.
All dimensions don't include mold flash & metal burr.

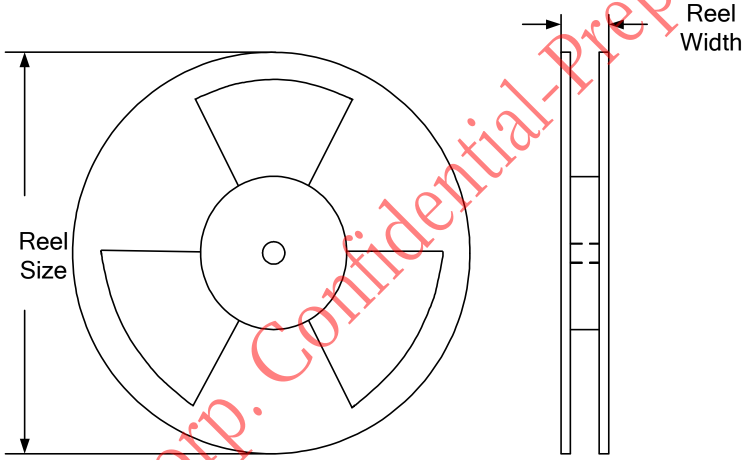
Taping & Reel Specification

1. Taping orientation for packages（SO8）



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Reel width(mm)	Trailer length(mm)	Leader length (mm)	Qty per reel
SOP8	12	8	13"	12.4	400	400	2500