PSR Flyback Controllers

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Agenda

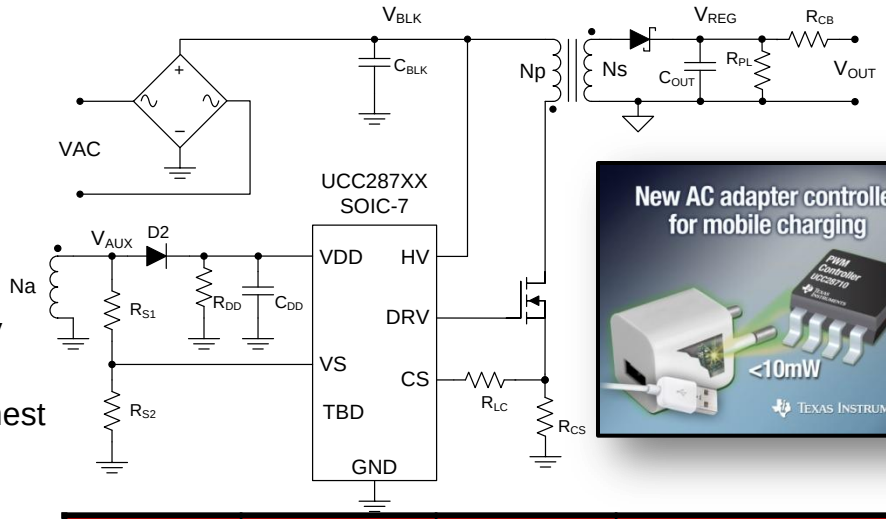
- Feature Overview
- Basic Control Methodology
  - Primary Side Voltage Regulation
  - Primary Side Current Regulation
- Controller Features
  - Performance Advantages
- Design Tips

UCC2871X Product Family

Constant Voltage, Constant Current PWM Controller with Primary-side Regulation

Features

- <10mW no load power (at 5-6W Pout)
- Internal 700V HV Start-up JFET
- Primary Side Regulation (PSR) eliminates opto-coupler
- +/- 5% Voltage & Current regulation
- 100 kHz max switching frequency enables high power density charger designs
- Different minimum frequency options to meet lowest cost/highest performance solution
- Quasi-resonant valley switching operation for highest overall efficiency
- Frequency jitter to ease EM I
- Wide VDD range (35V) allows small bias capacitor
- Drive Output for MOSFET
- Protection Functions: Over Voltage, Low Line & Over Current
- SOIC-7 Package



Part Number	Minimum Frequency	TBD Pin	No Load Power
UCC28710	680Hz	CBC	<10mW
UCC28711	680Hz	NTC/SD	<10mW
UCC28712	680Hz	NTC/SD	<10mW
UCC28713	680Hz	NTC/SD	<10mW
UCC28714	340Hz	CBC	<<10mW
UCC28715	1.5KHz	CBC	<30mW (1 o/p cap)

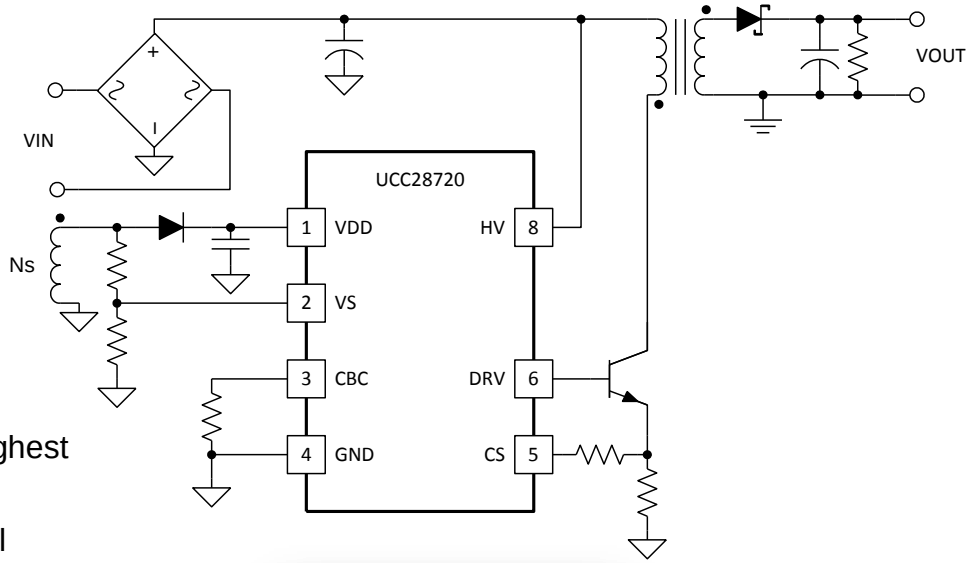
Applications

- Universal charging Solution AC Adapters
- Low Power AC/DC SMPS
- Power metering
- Auxiliary/Standby Power Supplies

Texas Instruments

UCC2872X Product Family

Constant Voltage, Constant Current PWM Controller with Primary-side Regulation



Features

- <10mW no load power (at 5-6W Pout)
- Internal 700V HV Start-up JFET
- Primary Side Regulation (PSR) eliminates opto-coupler
- +/- 5% Voltage & Current regulation
- 80 kHz max switching frequency enables high power densitycharger designs
- Different minimum frequency options to meet lowest cost/highest performance solution
- Quasi-resonant valley switching operation for highest overall efficiency
- Frequency jitter to ease EM I
- Wide VDD range (35V) allows small bias capacitor
- Drive Output for bipolar transistor - BJT
- Protection Functions: Over Voltage, Low Line & Over Current
- SOIC-7 (UCC28720) or SOT23-6 (UCC28722)

Applications

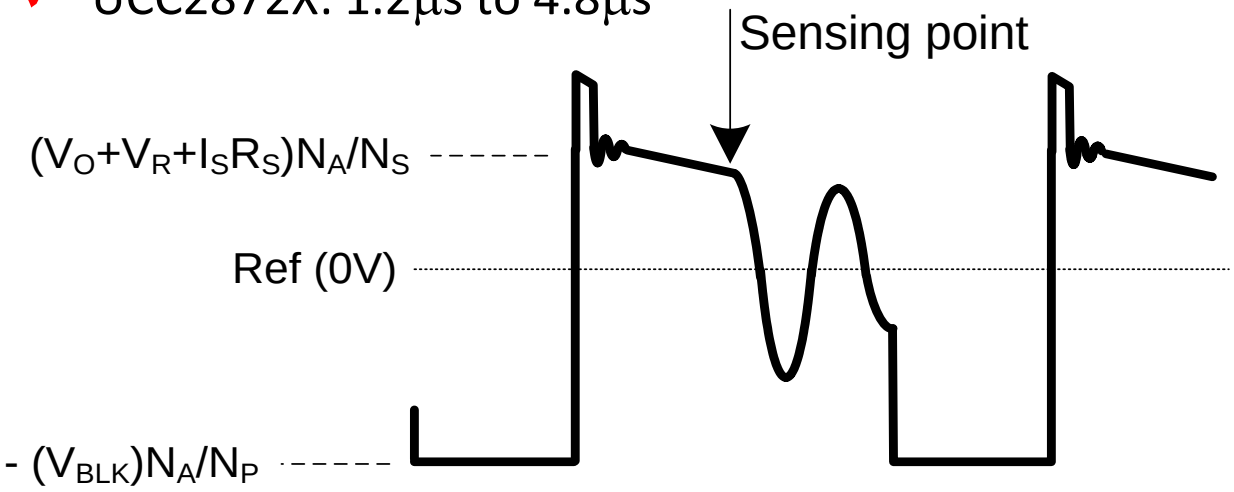
- Universal charging Solution AC Adapters
- Low Power AC/DC SMPS
- Power metering
- Auxiliary/Standby Power Supplies

Part Number	Startup	No Load Power
UCC28720	HV JFET	<10mW
UCC28722	Resistor	<50mW

Texas Instruments

Primary side Output Voltage Sensing

- ✓ Aux winding voltage sensed through resistor divider on VS pin
- ✓ Output voltage is sampled at end of secondary current conduction time
  - ✓ Eliminate IR voltage drop during conduction time of secondary current
  - ✓ VS signal discrimination to reject leakage current spike and ringing
  - ✓ Variable blanking time on VS pin for minimum and maximum current:
    - ✓ UCC2871X: 570ns to 1.7µs
    - ✓ UCC2872X: 1.2µs to 4.8µs



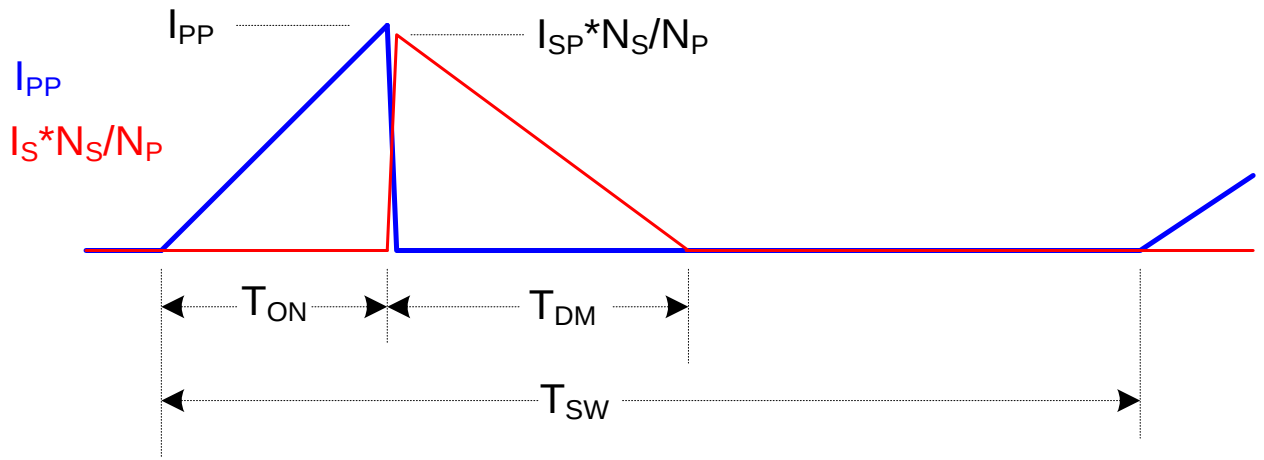
Aux winding voltage

Constant Output Voltage Regulation

- ✓ Control output voltage to achieve +/-5% voltage regulation meeting USB standard requirement
- ✓ Precise internal reference to tight regulation
  - ✓ VS internal 4V reference with +/-1% accuracy
- ✓ Temperature compensation for output rectifier voltage drop
  - ✓ 0.8mV/^{o}C on VS reference, equates to ~1.1mV/^{o}C on Sec winding
  - ✓ With 5:1 VS resistor divider, 1% resistors, divider worst case tolerance dominates at 1.6%
- ✓ Optional cable compensation available

Primary side Control Constant Current Regulation

- ✓ **+/-5% Constant Current Regulation**
  - √ Primary Side Current Regulation
    - √ CC regulation based on Ipri Pk and demag time duty cycle (T_{DM}/T_{SW})
    - √ CC regulation occurs at Ipri Pk max. Constant current regulation loop occurs When T_{DM}/T_{SW} is 42.5%. As Vout is reduced, Fsw is reduced to maintain constant TDM duty cycle of 42.5%.

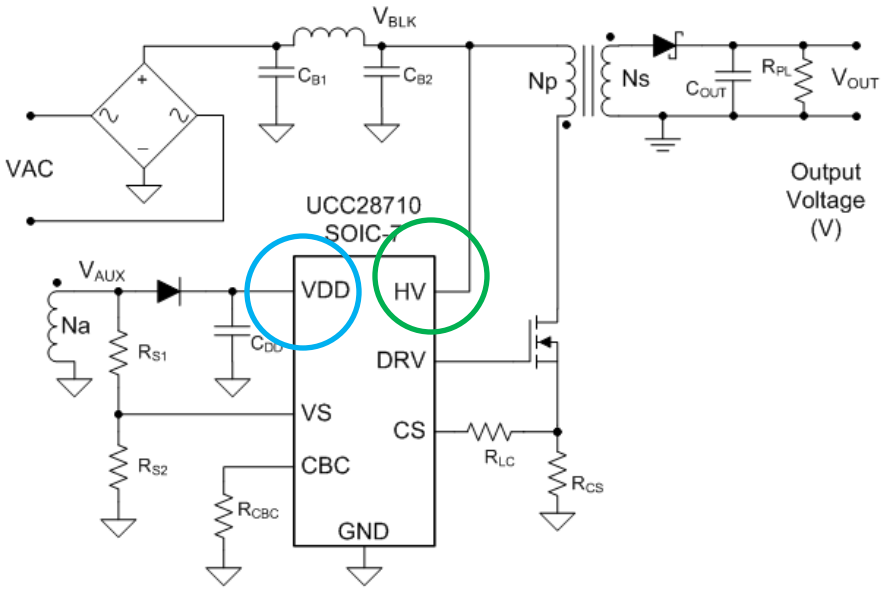


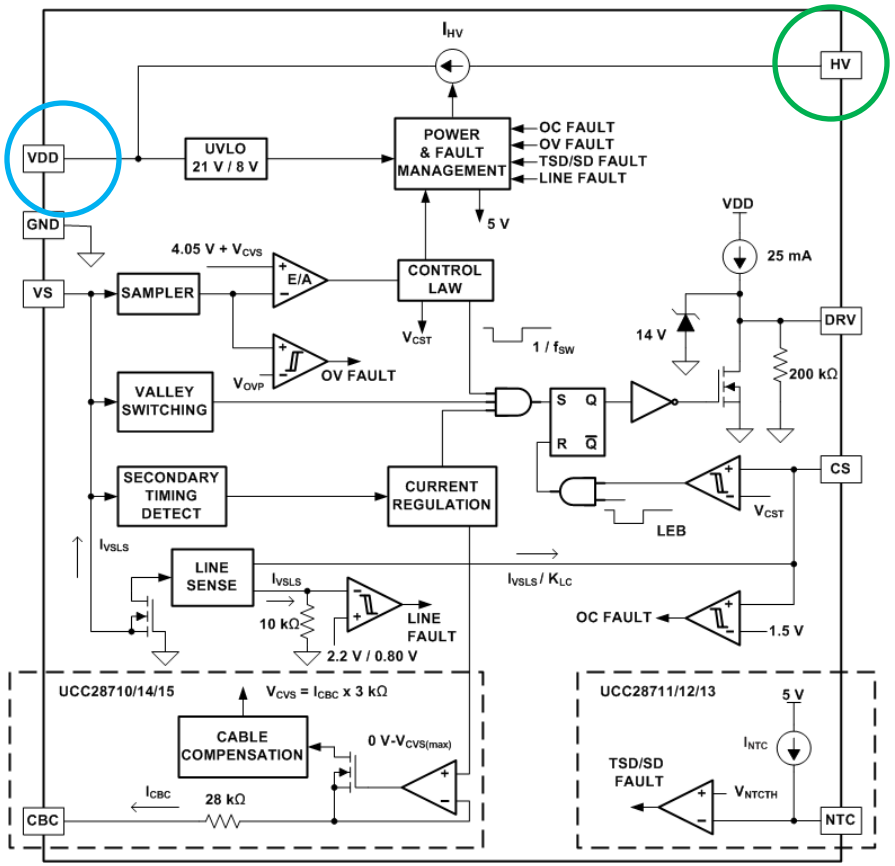
$$I_{OUT} = ½ (I_{SP}) * T_{DM}/T_{SW}$$

$$I_{OUT} = ½ (I_{PP}*N_P/N_S) * T_{DM}/T_{SW}$$

Device Features: HV & VDD Pins

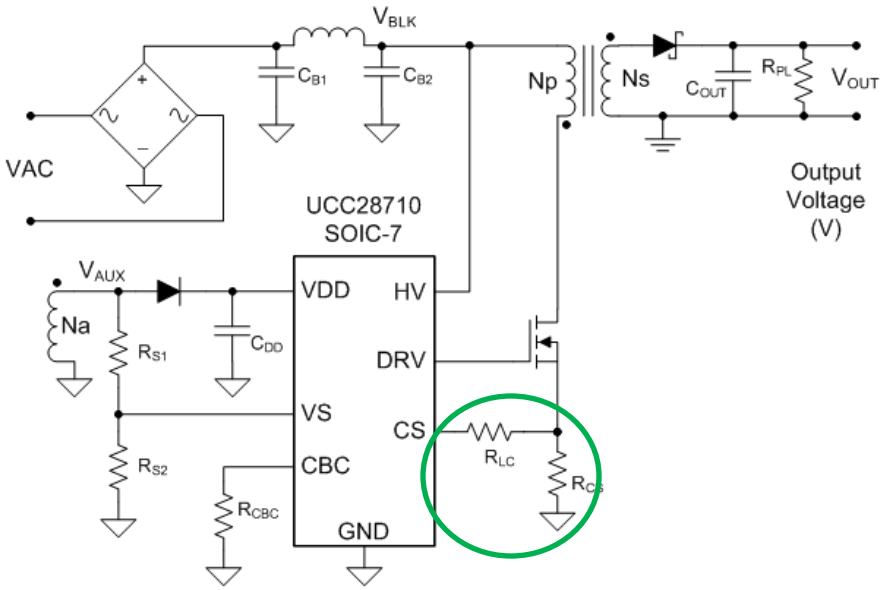
Startup, UVLO

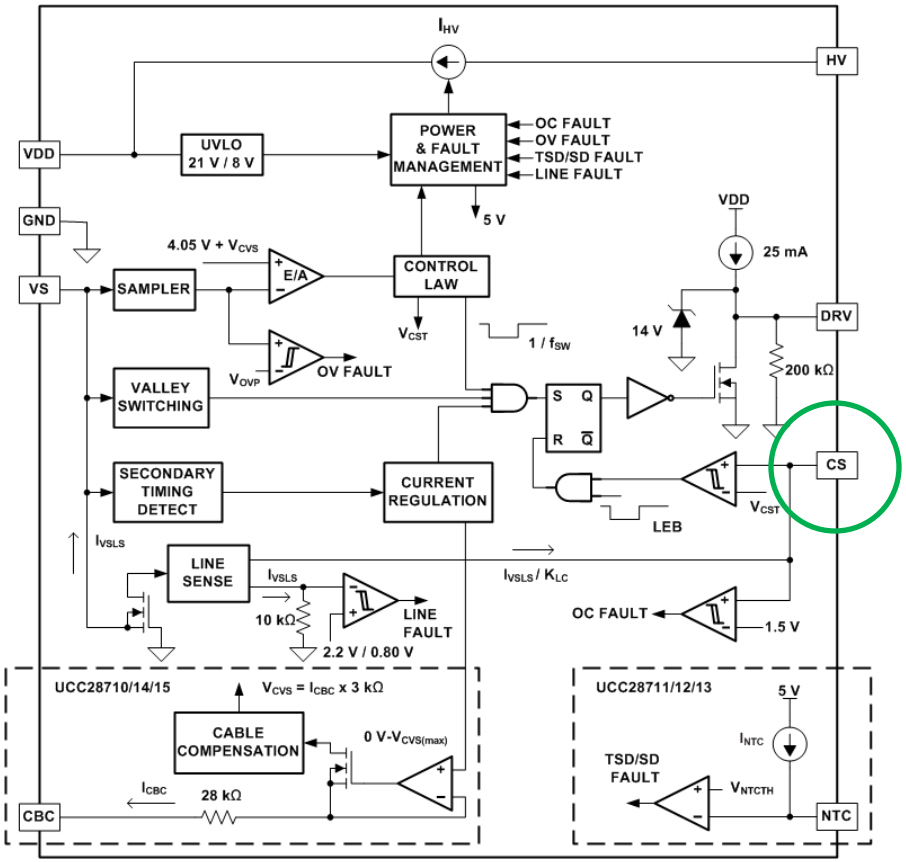




- ✓ IC HV startup current: 250uA typical
- ✓ UVLO Turn-on 21V, Turn-off 8.1V
  - Allows small V_{DD} capacitance

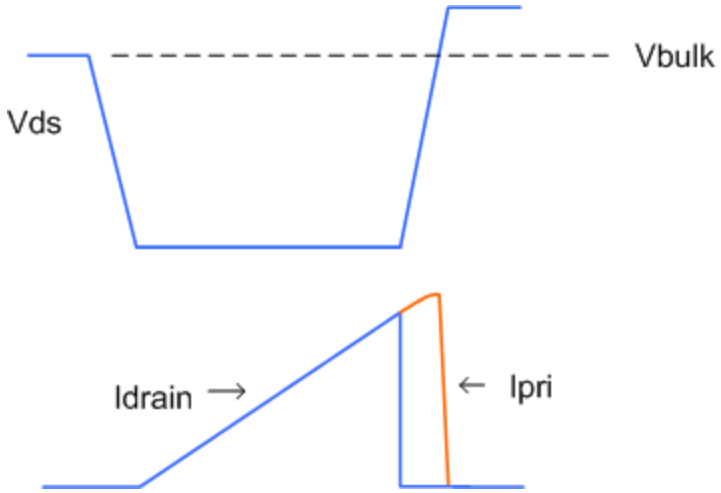
Device Features: CS Pin I_{PRI} Control and Fault



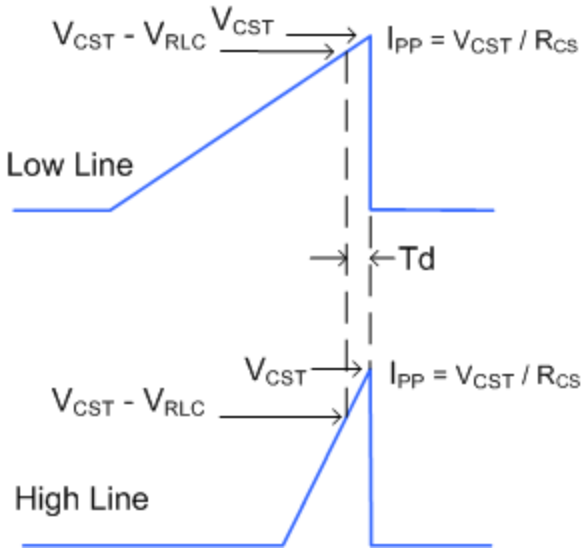


- ✓ I_{PRI} sensing:
  - ✓ Control peak current (0.19V to 0.78V) during regulation
  - ✓ Over current fault (1.5V)

Device Features: CS Pin I_{PRI} Feedforward with Line



Real peak current is higher than expected

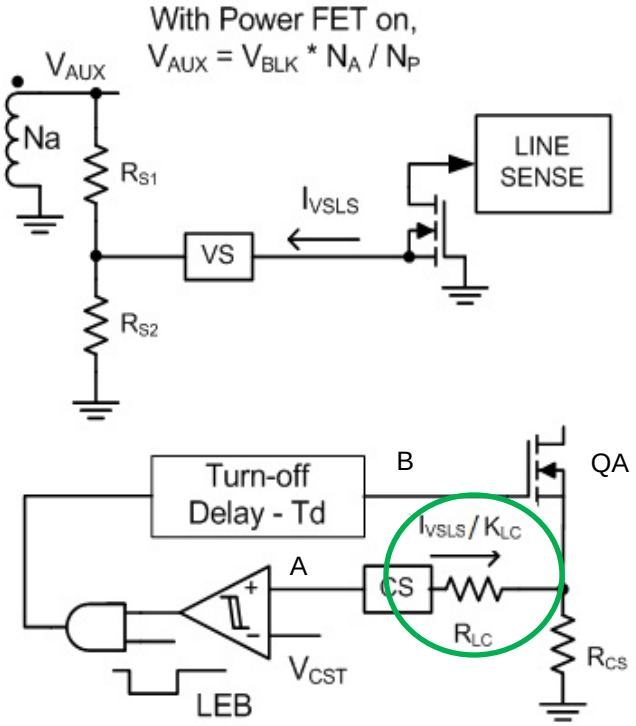


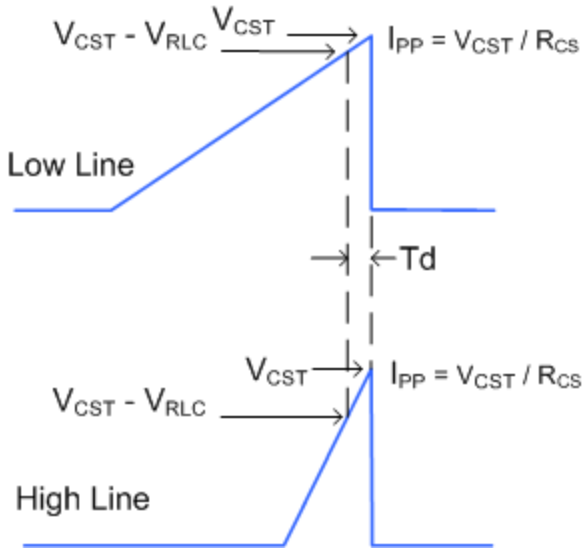
Peak current error is proportional to line voltage

- √ Line Compensation results in excellent CC regulation over line range
  - √ CC regulation based on primary side peak current and de-magnetizing time duty cycle
  - √ Compensate IC internal delay and gate drive turn off delay to control Ipri Pk over line range
  - √ Compensate for additional transformer primary peak current due to MOSFET Vds turn off rise time. MOSFET dv/dt determined by Ipri and total drain capacitance.

Device Features: CS Pin
I_{PRI} Feedforward with Line

- ✓ **Adds offset to the CS signal**
  - ✓ **Provides increasing offset with increasing line, program with R_{LC} value**
  - ✓ **Current out of CS pin is 1/25 of current in VS pin during MOSFET on time.**

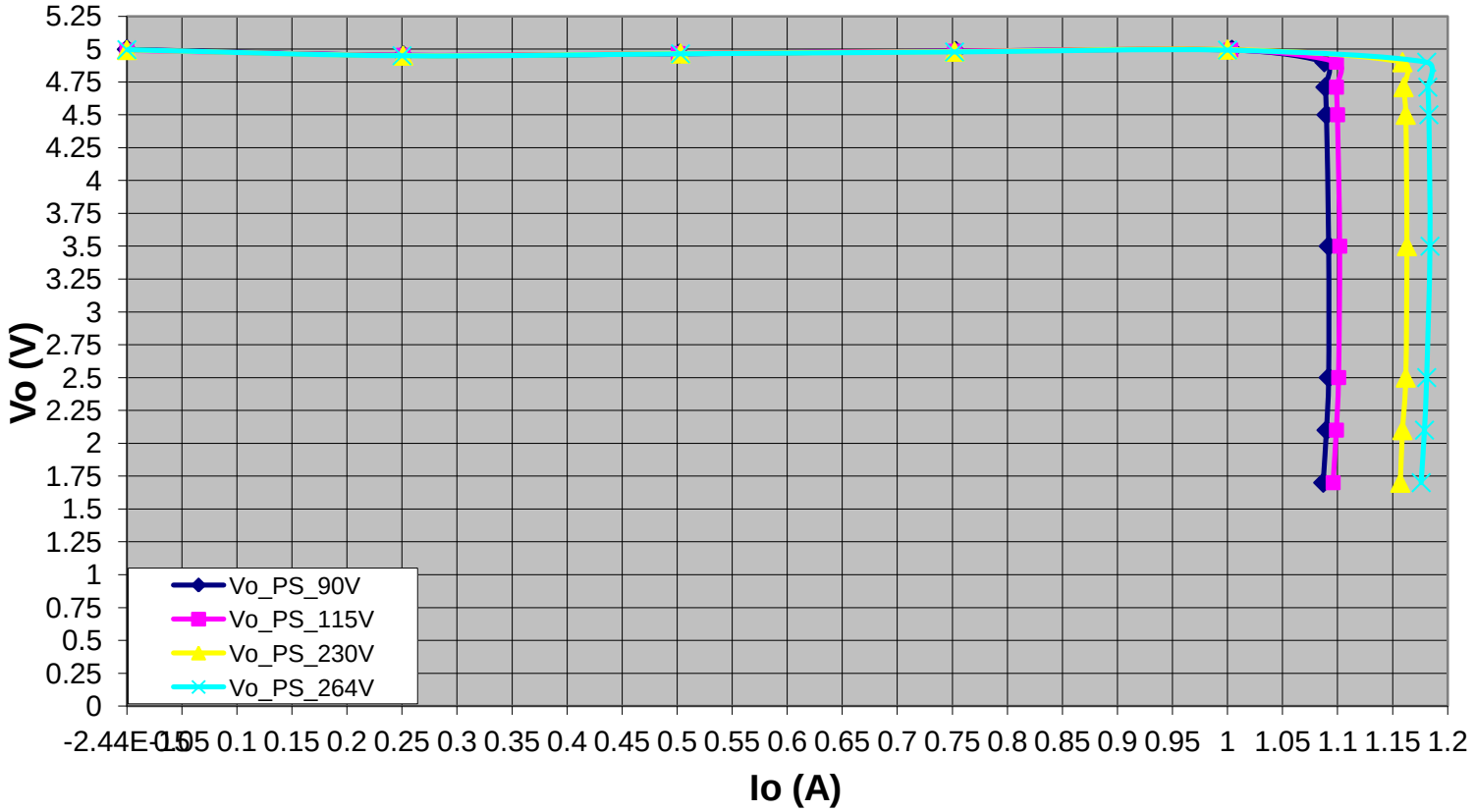




$$R_{LC} = \frac{K_{LC} \times R_{S1} \times R_{CS} \times t_d \times N_{PA}}{L_P}$$

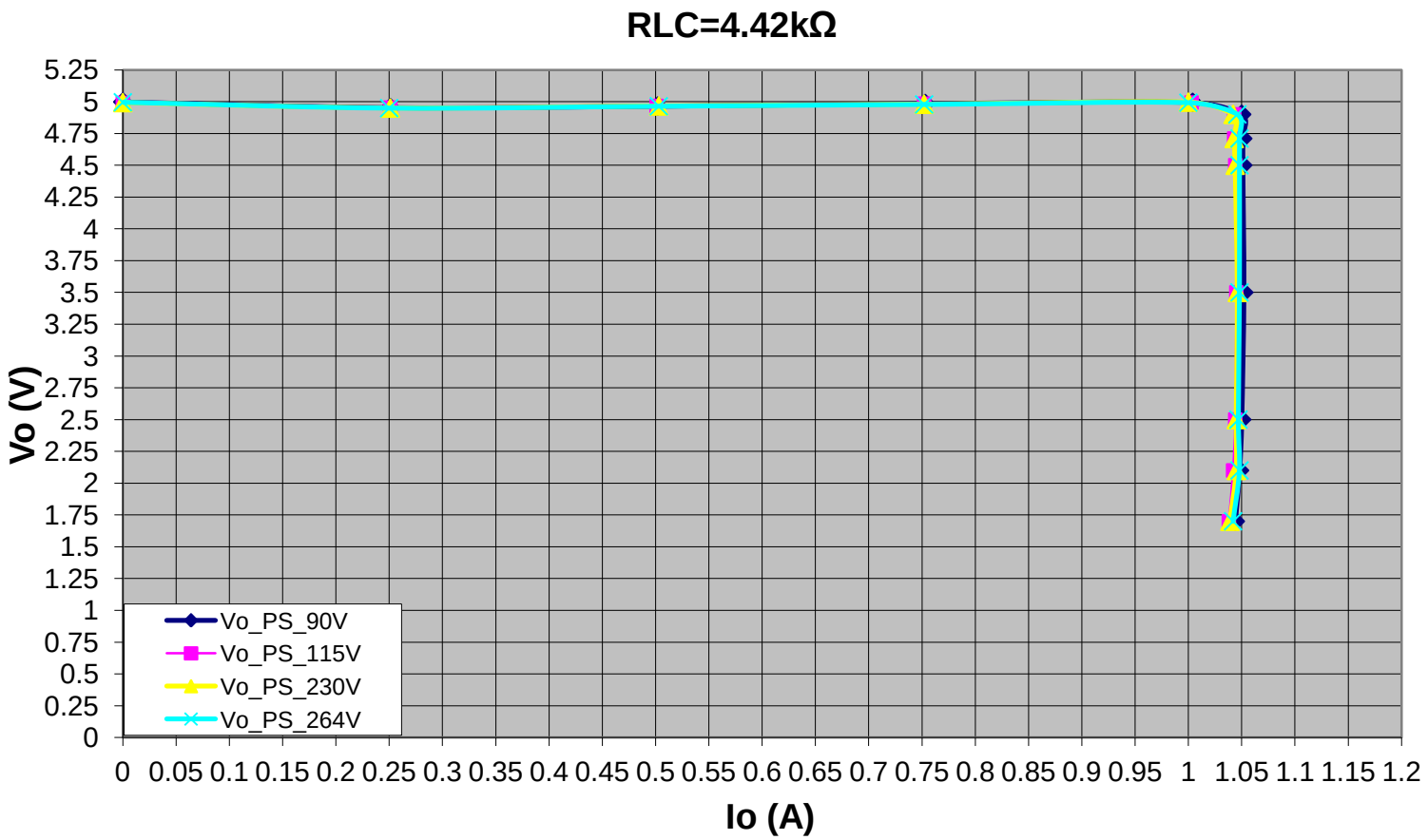
I_{PRI} Feedforward with Line: Benefit Constant Current without Line Compensation

- √ V/I Curve of with Line Compensation resistor at 0 Ohms (No Line Compensation).
  - √ CC regulation +4/-4%: 90V to 264VAC and Vout from 4.7 to 2V.

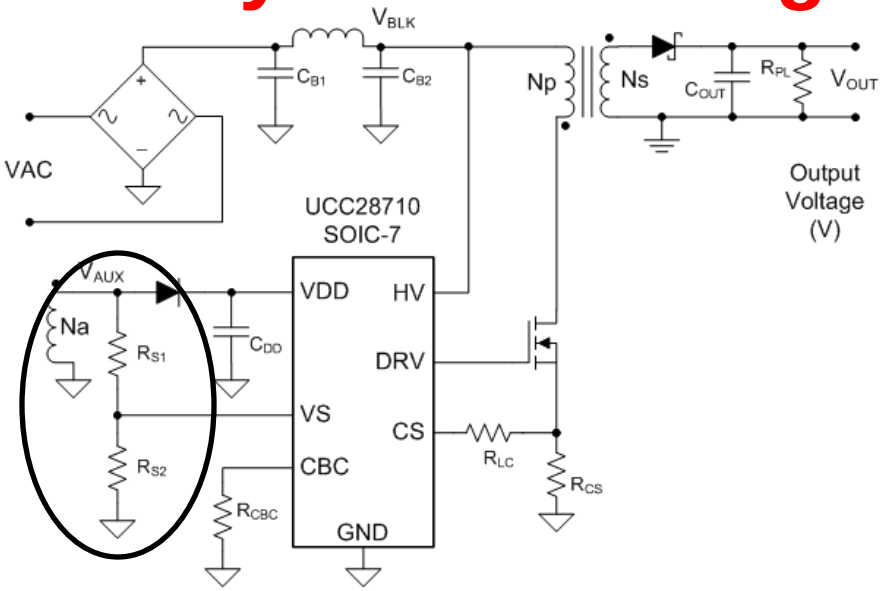


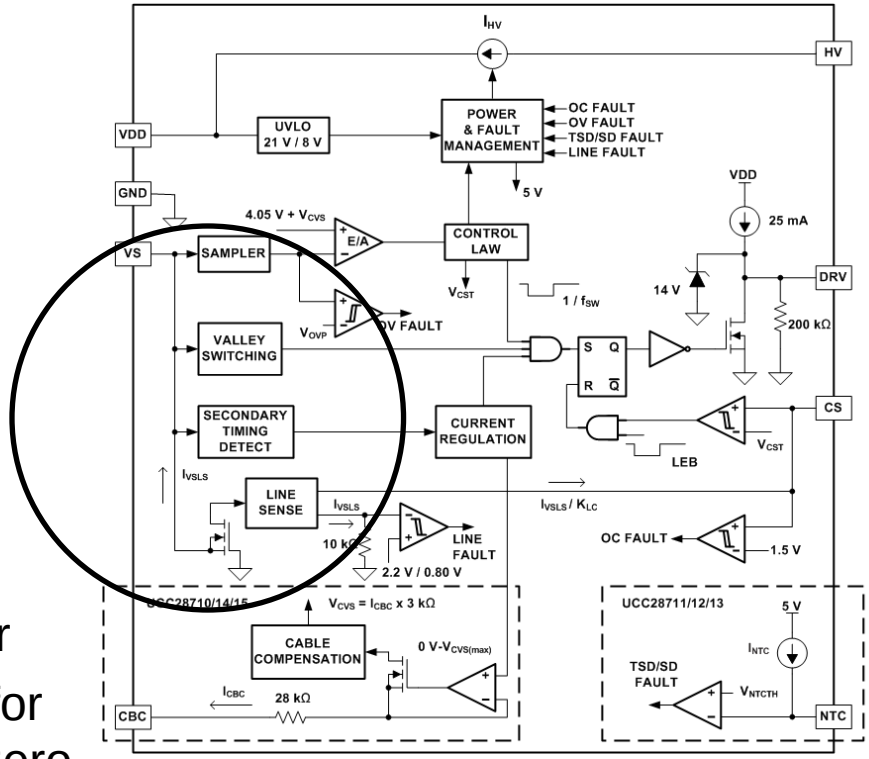
I_{PRI} Feedforward with Line: Benefit Constant Current with Line Compensation

- √ V/I Curve of With Line Compensation resistor selected
  - √ CC regulation +0.5/-0.8% : 90V to 264VAC and Vout from 4.7 to 2V.



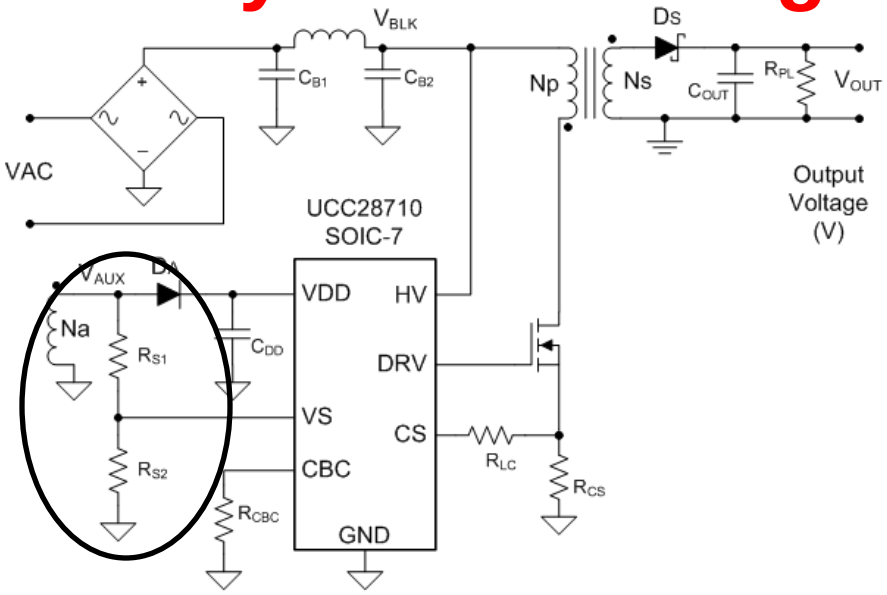
Device Features: VS Pin Primary Aux Sensing





- ✓ Eliminates the need for an opto isolator
- ✓ Detects Zero Current to initiate timing for voltage or current regulation. Detects zero voltage to initiate valley switching.
- ✓ N_S/N_A and R_{S2}/R_{S1} ratio controls
  - ✓ Output Voltage (V_{OUT})
  - ✓ Input Voltage Enable ($V_{IN\_(run)}$)
  - ✓ Output Over Voltage Protection (V_{OVP})

Device Features: VS Pin Primary Aux Sensing



- ✓ Primary Aux Sensing (VS) $N_{AS}=N_A/N_S$ and $N_{PA}=N_P/N_A$ Controls
  - ✓ Output Voltage (V_{OUT})
  - ✓ AC Input Enable ($V_{IN(run)}$)
  - ✓ Output Over Voltage Protection (V_{OVP})

The high side resistor and N_P/N_A ratio determines AC line turn on voltage

$$I_{VSL(run)} \approx 225uA$$

$$R_{S1} = \frac{V_{IN(run)} \times \sqrt{2}}{N_{PA} \times I_{VSL(run)}}$$

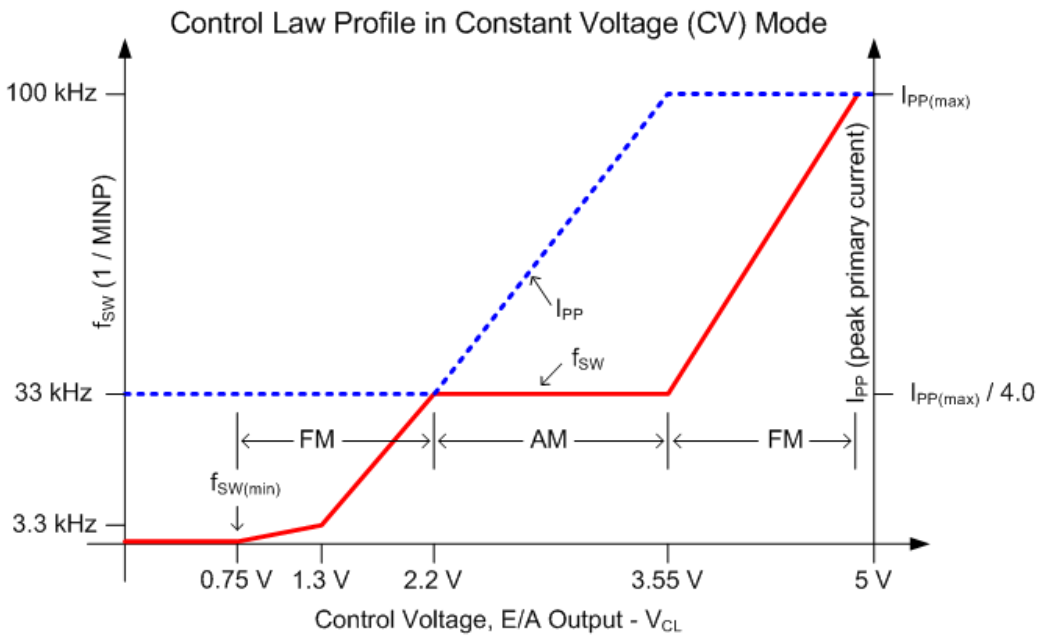
The resistor divider N_A/N_S ratio determine V_{OUT}

$$V_{VSR} = 4.05V \qquad V_{OVP} = 4.60V$$

$$R_{S2} = \frac{R_{S1} \times V_{VSR}}{N_{AS} \times (V_{OUT} + V_{FS}) - V_{VSR}}$$

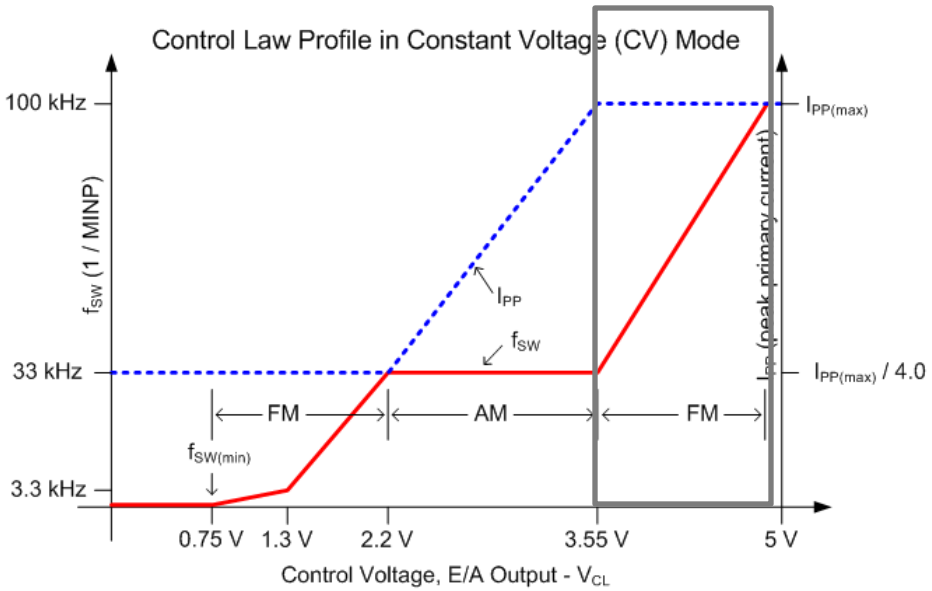
Note: V_{FS} is the secondary diode V_F at very low current

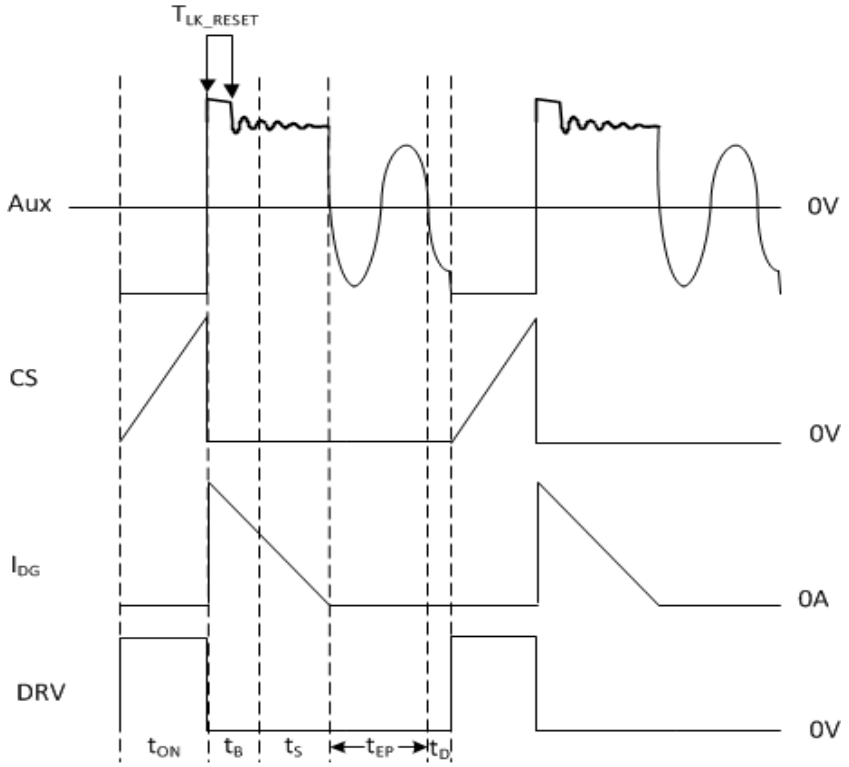
Voltage Regulation Control Law: Frequency and I_{PRI}



- ✓ Combination of frequency modulation, and peak current modulation
  - ✓ Extended PFM modulation results in wide dynamic range, 2300 to 4700
    - ✓ UCC28711: Fswmin 680Hz, 2300
    - ✓ UCC28714: Fswmin 340Hz, 4700
    - ✓ UCC2872X: Fswmin 650Hz (28kHz f_{SW} during AM range)
  - ✓ Frequency modulation results in flat efficiency curve.

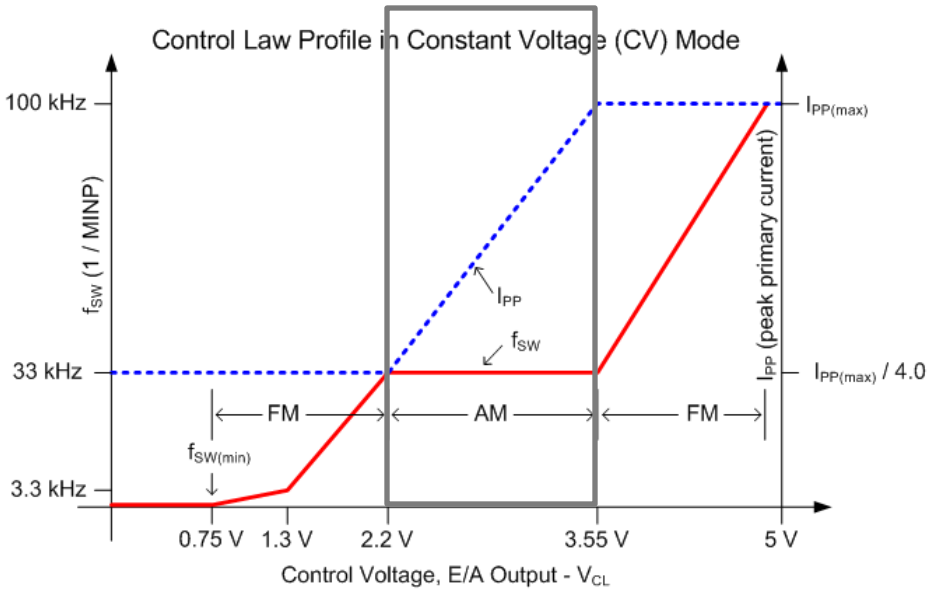
Voltage Regulation Control Law: Frequency and I_{PRI}

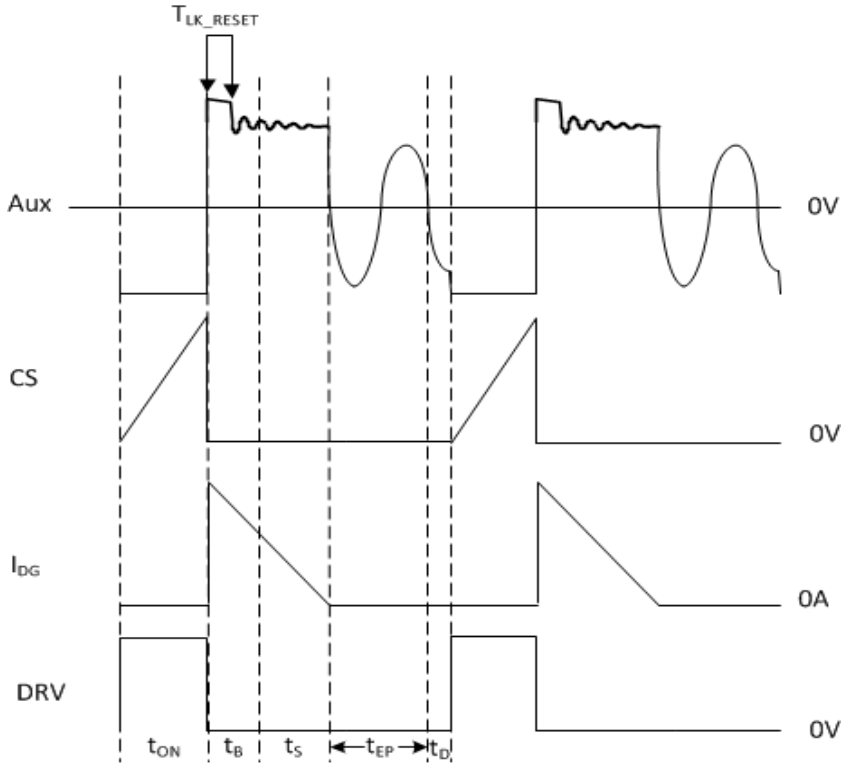




- ✓ $V_{E/A}$ 3.55V to 5V, V_{RCS} = 0.78V
  - ✓ I_{PRI} set at Max
    - ✓ Transformer designed to Transition mode limit at max power and minimum Vin.
  - ✓ A delay is added/adjusted (t_{EP}) to adjust frequency (33 kHz to 100 kHz (IC limit))
  - ✓ Controller will not turn on DRV until VS zero voltage is detected and t_D has timed out (150ns UCC281X, 300ns UCC2812X)
    - ✓ This achieves valley switching

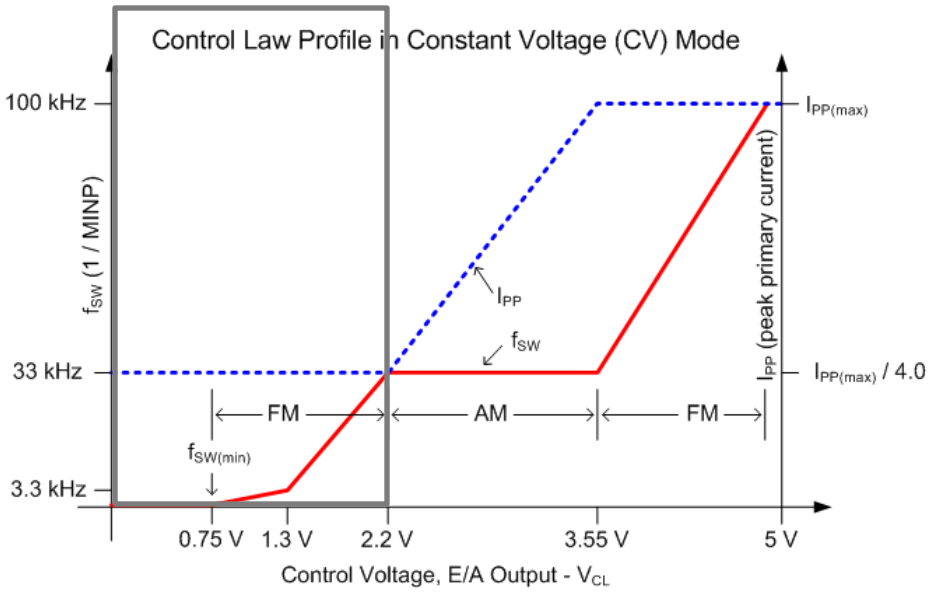
Voltage Regulation Control Law: Frequency and I_{PRI}

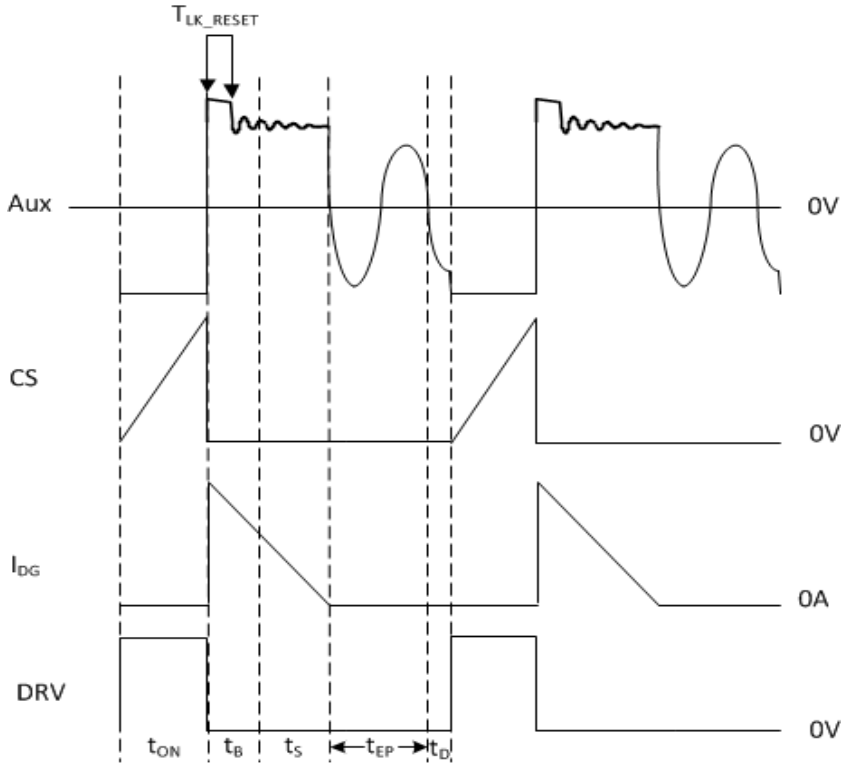




- ✓ VE/A 2.2V to 3.55V, VCS = 0.19V to 0.78V
  - ✓ Converter is operating deeper into DCM
  - ✓ Frequency is Fixed 33 kHz (28kHz for UCC2872X)
  - ✓ Power is Controlled by Adjusting CS amplitude (AM) from IPP(max) to 1/4 IPP(max)
    - ✓ Valley switching as long as can be detected

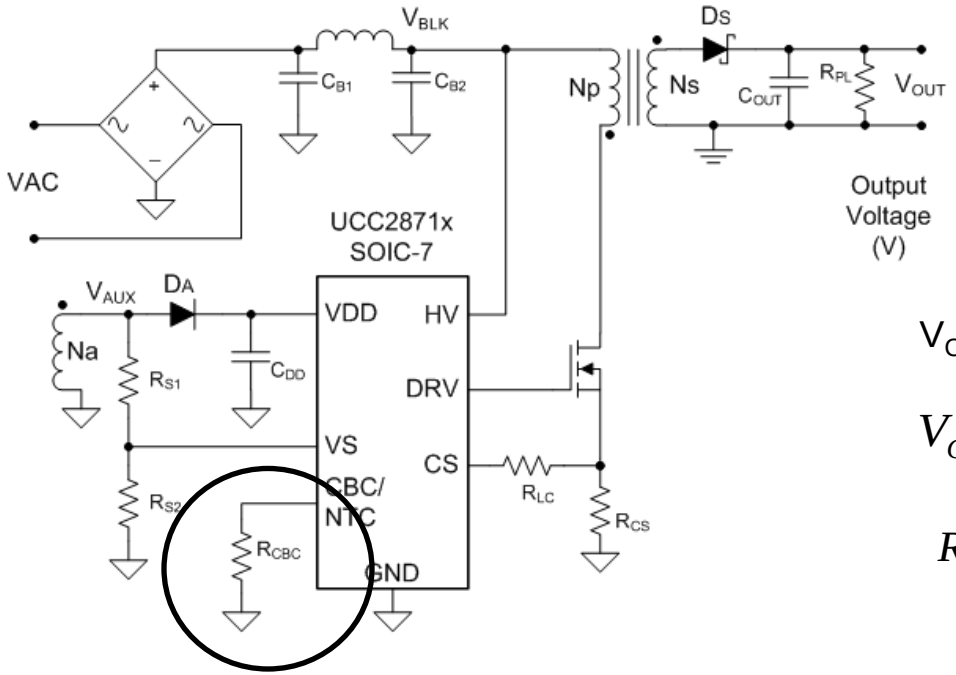
Voltage Regulation Control Law: Frequency and I_{PRI}



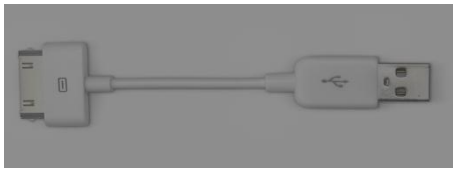


- ✓ VE/A 0.75V to 2.2V, V_{RCS} = 0.19V
  - ✓ Power is Controlled by adjusting t_{EP} at IPP(max)/4
  - ✓ Frequency is adjust from 33 kHz down to 680 Hz depending on E/A out
  - ✓ IPP is fixed to 1/4 IPP MAX
  - ✓ When E/A drops below 0.75V frequency is fixed at Fswmin
    - ✓ Fswmin: 340Hz (UCC28714), 680Hz (UCC28710-13), 1.4kHz (UCC28715), 650Hz (UCC2872X)

Device Features: CBC Pin - Cable Compensation, UCC28710/14/15, UCC2872X



V_{CBC}= I*R



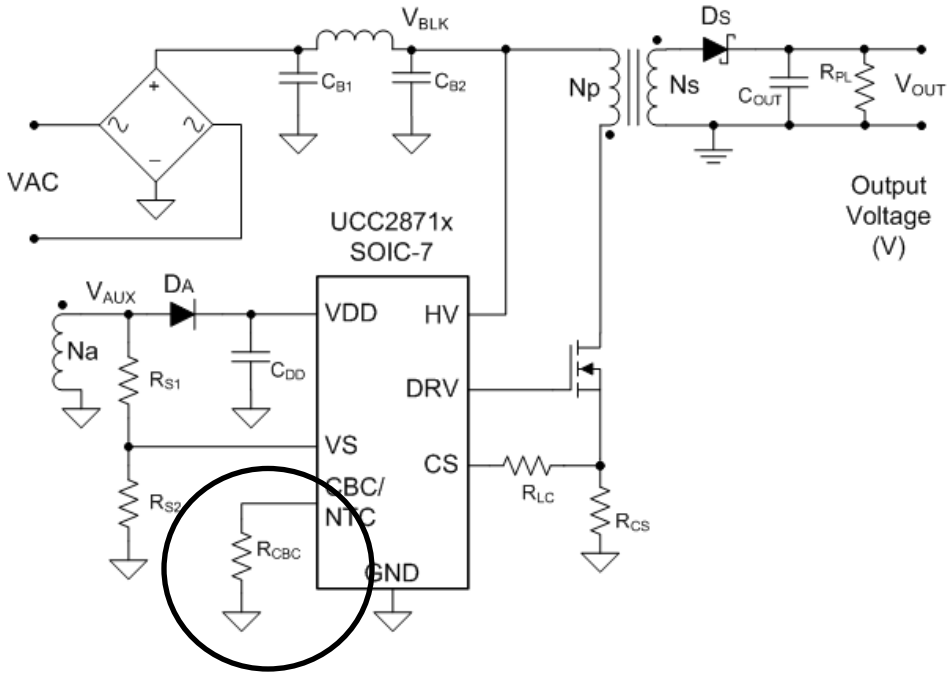
V_{CBCM} = V @ CBC (Pin3) V_{VSR} = VS Reg. Point

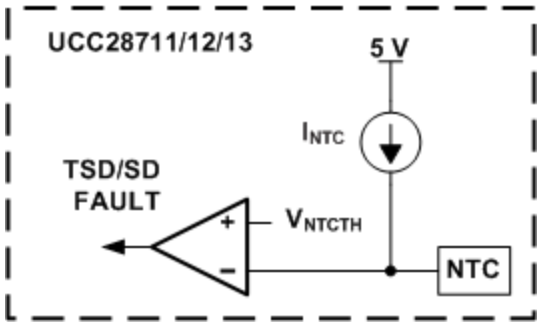
$$V_{CBCM} \approx 3V \qquad V_{VSR} \approx 4.05V$$

$$R_{CBC} = \frac{V_{CBCM} \times 3k\Omega \times (V_{OUT} + V_{DS})}{V_{VSR} \times V_{CBC}} - 28k\Omega$$

- ✓ Devices have a cable compensation adjustment (R_{CBC})
  - ✓ Compensates the IR drop from the cable
    - ✓ Moves with load
    - ✓ Maximum cable compensation with R_{CBC} low
    - ✓ Minimum cable compensation with R_{CBC} open

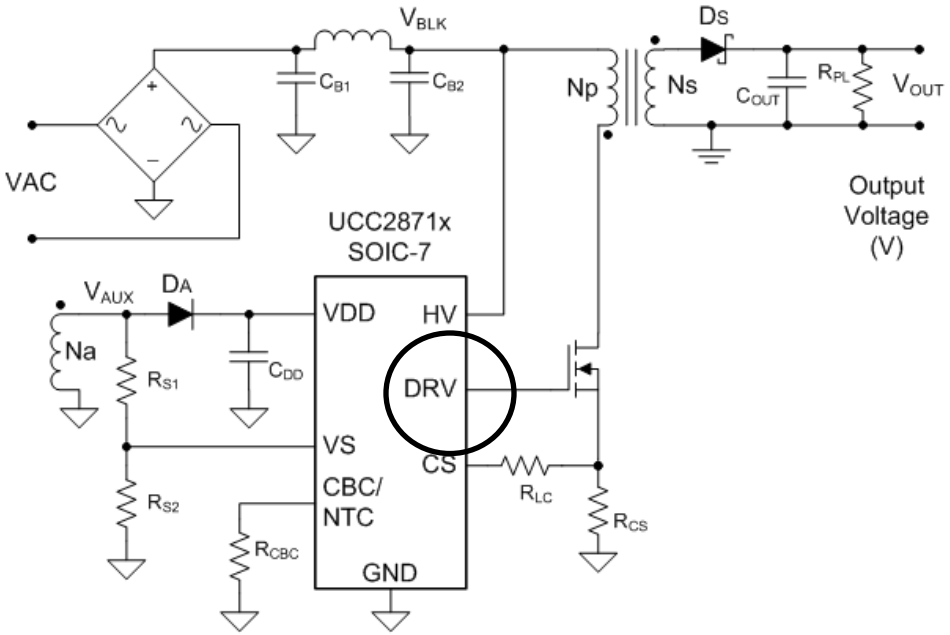
Device Features: NTC Pin
NTC Shutdown, UCC28711/12/13

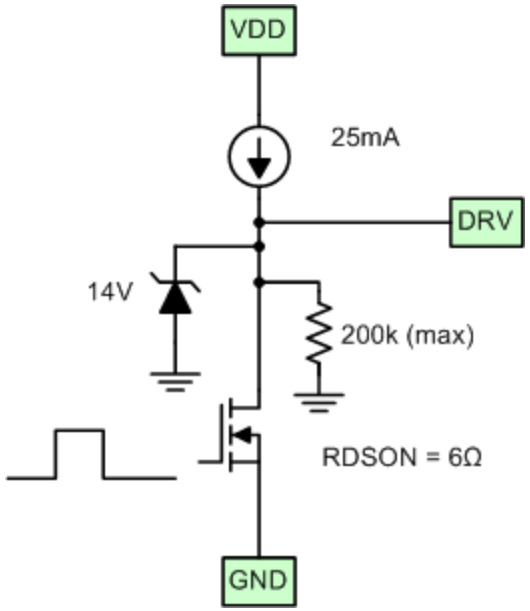




- ✓ UCC28711/12/13 has a pin for an NTC thermistor
  - ✓ Programmable Thermal Shutdown
  - ✓ Pin sources 105 uA (I_{NTC})
  - ✓ Part shuts down when less than 0.95V (V_{NTCTH})

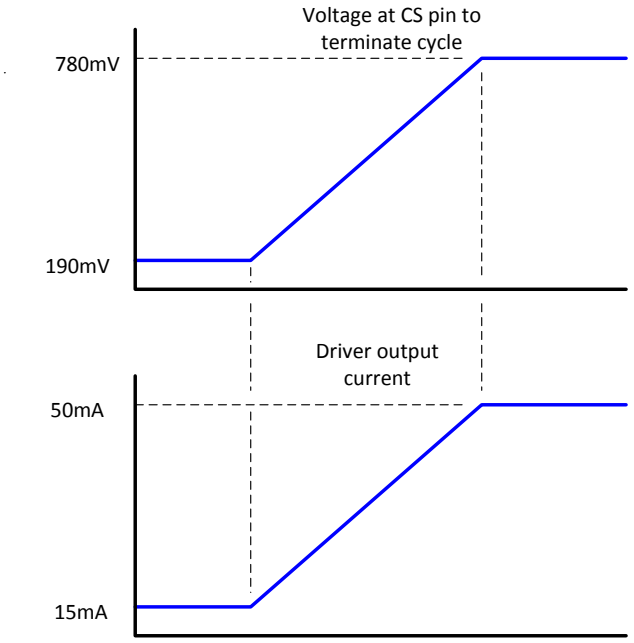
Device Features: DRV Pin UCC2871X Gate Drive

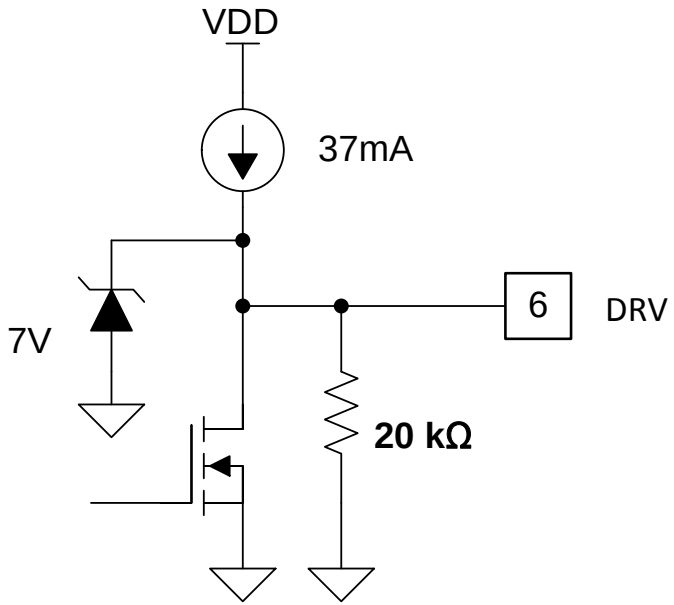




- ✓ Gate Drive
  - ✓ Internal gate pulldown resistance
  - ✓ DRV limited to 14V
  - ✓ Current source turn on to limit MOSFET turn on dV/dt
  - ✓ Turn off 6Ω low side switch

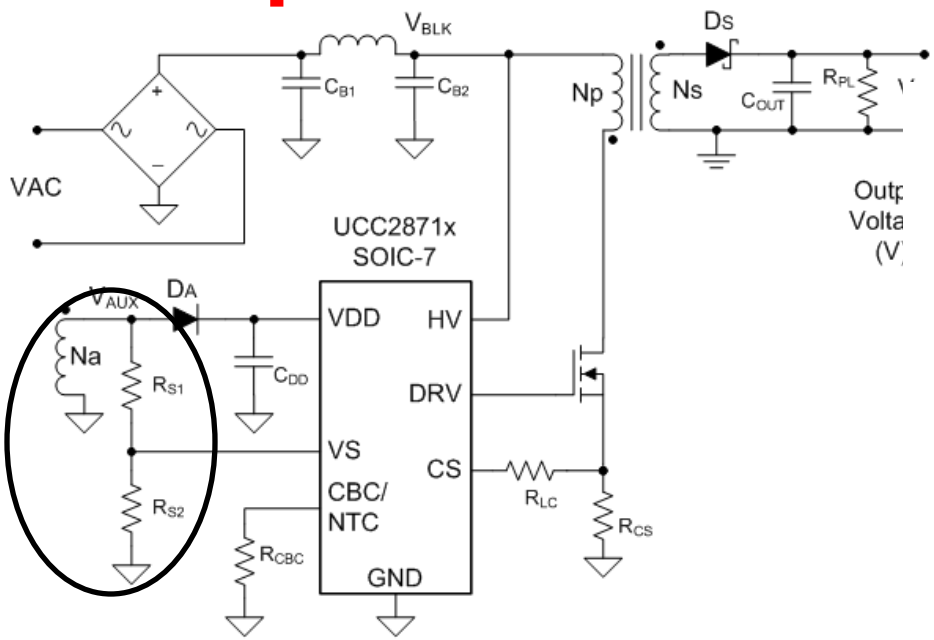
Device Features: DRV Pin UCC2872X Gate Drive



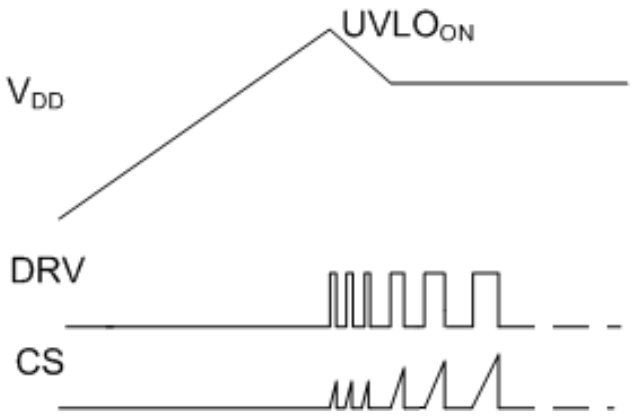


- ✓ Gate Drive
  - ✓ Internal gate pulldown resistance, 20kΩ
  - ✓ DRV limited to 6V
  - ✓ Current source output for driving bipolar transistor base
  - ✓ Drive current varies as peak current varies to optimize transistor drive and
  - ✓ minimize storage time
  - ✓ Turn off 1Ω low side switch

Startup/Fault



Normal Startup

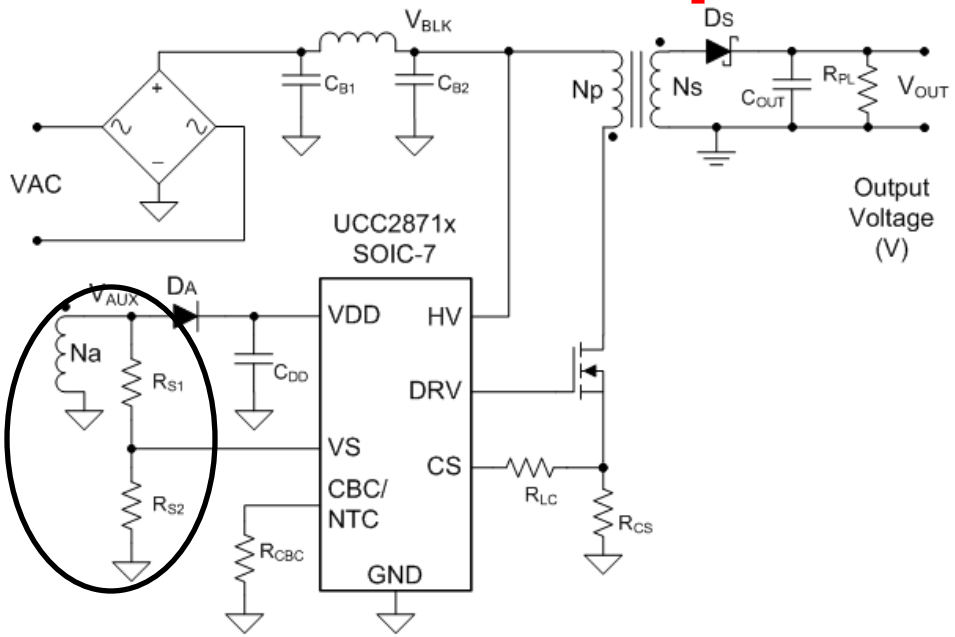


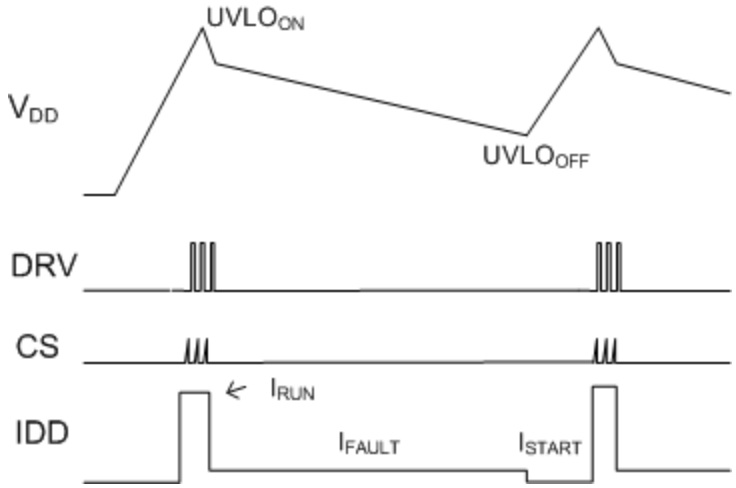
- ✓ Sequence:
  - ✓ VDD charged through HV startup switch to 21V ($UVLO_{ON}$)
    - ✓ Fast start up
  - ✓ 3 gate driver pulses are initiated @ $UVLO_{ON}$ at 1/4 IPPmax
  - ✓ If no fault detected, control law dictates operation
  - ✓ If fault is detected switching stops and UVLO is initiated

Faults that Initiate UVLO

- ✓ Output over-voltage: V_{OUT} > 115% Target (4.6V on VS pin)
- ✓ Input under-voltage (IVS < IVL(run) or (stop))
  - ✓ Start current on VS pin is 225uA, stop current is 80uA
- ✓ Internal over-temperature(> 165 ^{o}C J_T)
- ✓ Primary over-current (CS > 1.5V)

Fault UVLO Sequence





- ✓ Fault Sequence:
  - ✓ All faults require 3 events to initiate UVLO recycle.
    - ✓ After 3 fault cycles, switching stops
    - ✓ IC goes to I_{FAULT} (95uA) draw on V_{DD} cap
    - ✓ When V_{DD} reaches 8V $UVLO_{OFF}$, restart sequence begins with HV switch enable
    - ✓ V_{DD} capacitance and I_{FAULT} determine fault cycle time
  - ✓ All faults recycle and restart

Design Tips and Recommendations

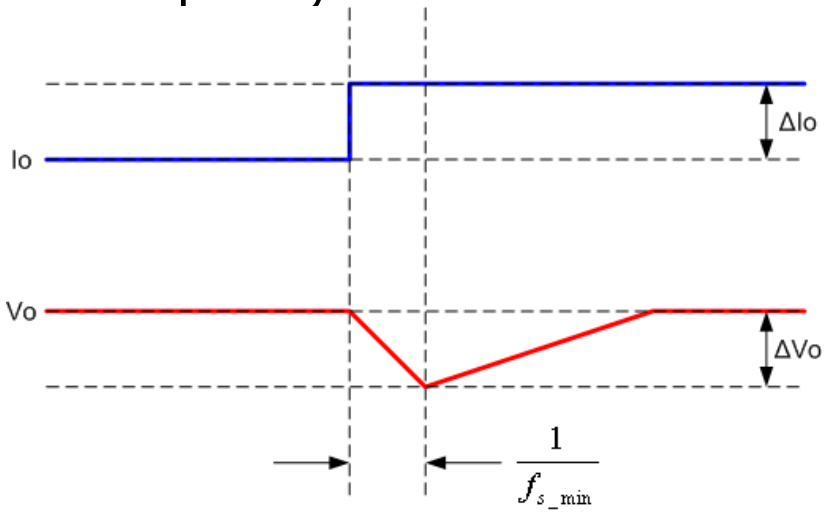
- ✓ PSR Limitations on load transient, output capacitance value.
  - ✓ With PSR the output can only be sampled at the Fsw.
    - ✓ At no load to load transient, output will not be sampled until next cycle.
- ✓ Determining basic transformer parameters

Design Tips and Recommendations

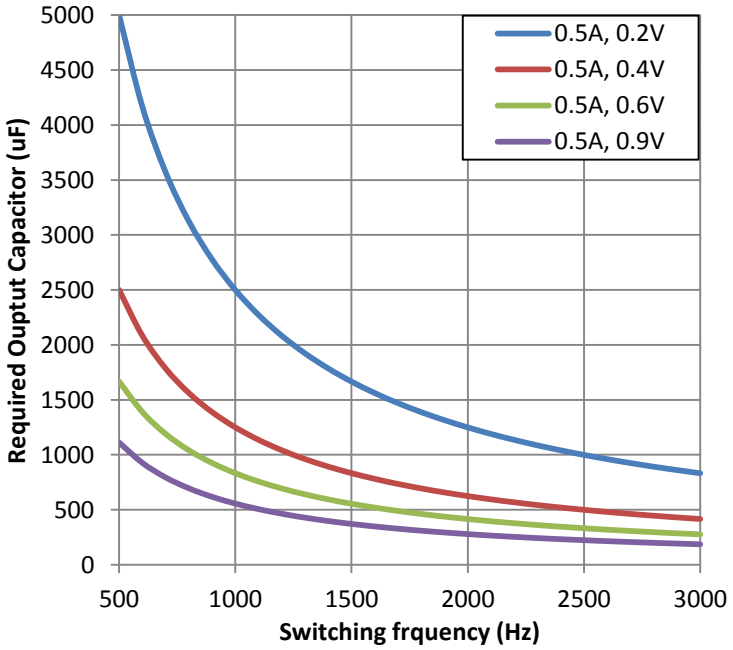
- ✓ Common Problems With PSR Flyback Designs
  - ✓ Excessive low frequency ripple on Vout, usually at lighter loads
  - ✓ Vout regulation at no load, high line
  - ✓ V/I Curve: Voltage out of regulation before Constant Current limit
  - ✓ Standby (no load) power too high

Design Tips and Recommendations
Tradeoff between Standby Power and Transient

- ✓ Standby power can be further improved by lower switching frequency but limited by transient response
- ✓ Due to the primary side control, the output voltage is only sensed after switching
- ✓ Worst transient response happens at the minimum switching frequency



$$C_{OUT} = \frac{\Delta I_o}{\Delta V_o \times f_{s\_min}}$$



To keep reasonable output capacitor value ~820uF, the minimum switching frequency is selected as 680Hz

Design Tips and Recommendations
Determine Transformer Parameters

- ✓ Example will assume a 5V charger targeting USB specs: Constant current source to 2V.
- ✓ The minimum voltage on the bulk capacitors has been calculated.
- ✓ Turns ratios

$$D_{MAG} = 0.425$$

Maximum secondary duty cycle
Set in IC

$$D_{MAX} = 1 - D_{MAG} - \frac{Tr \times F_{MAX}}{2}$$

Determine primary max duty cycle.
Tr is DCM resonant frequency
F_{MAX} is target Fsw of converter at full load

$$N_{PS} = \frac{D_{MAX} \times V_{BULK(\min)}}{D_{MAG} \times (V_{OUT} + V_{FS} + V_{CBC})}$$

Maximum primary to secondary turns ratio
V_{FS} is secondary rectifier forward drop
V_{CBC} is cable compensation votlage

$$N_{AS} = \frac{V_{DD(off)} \times V_{FA}}{V_{OUTCC} + V_{FS}}$$

Aux to secondary turns ratio
V_{FA} is aux rectifier forward drop
V_{OUTCC} is minimum Vout target in const current limit.

Design Tips and Recommendations
Determine Transformer Parameters

- ✓ Turns ratios from before.
- ✓ Determine I_{PRI} based on N_{PS} and CC target
- ✓ Inductance based on standard equation
- ✓ Check $t_{on(min)}$ and $t_{DMAG(min)}$, target 300ns and 1.2us

$$I_{PRI\_PK} = 2 \times \frac{I_{OUTCC}}{D_{MAG} \times N_{PS}}$$

At constant current limit, N_{PS} and primary current determine I_{OUT} average. $D_{MAG} = 0.425$

$$L_{PRI} = \frac{\frac{2 \times (V_{OUT} + V_{FS} + V_{CBC}) \times I_{OUTCC}}{\eta_{XFMR}}}{I_{PRI\_PK}^{2} \times F_{MAX}}$$

η_{XFMR} is transformer efficiency including leakage, core/copper loss, and bias power. 0.9 is good assumption.
V_{FS} is secondary rectifier forward drop
V_{CBC} is cable compensation voltage

$$t_{ON(\min)} = \frac{L_{PRI} \times I_{PRI\_PK} \times V_{CST(\min)}}{V_{IN(\max)} \times \sqrt{2} \times V_{CST(\max)}}$$

$V_{CST(min)}$ is minimum CS threshold.
$V_{CST(max)}$ is maximum CS threshold.

$$t_{DMAG(\min)} = \frac{t_{ON} \times V_{IN(\max)} \times \sqrt{2}}{N_{PS} \times (V_{OUT} + V_{FS})}$$

t_{ON} is primary on time at minimum CS threshold.

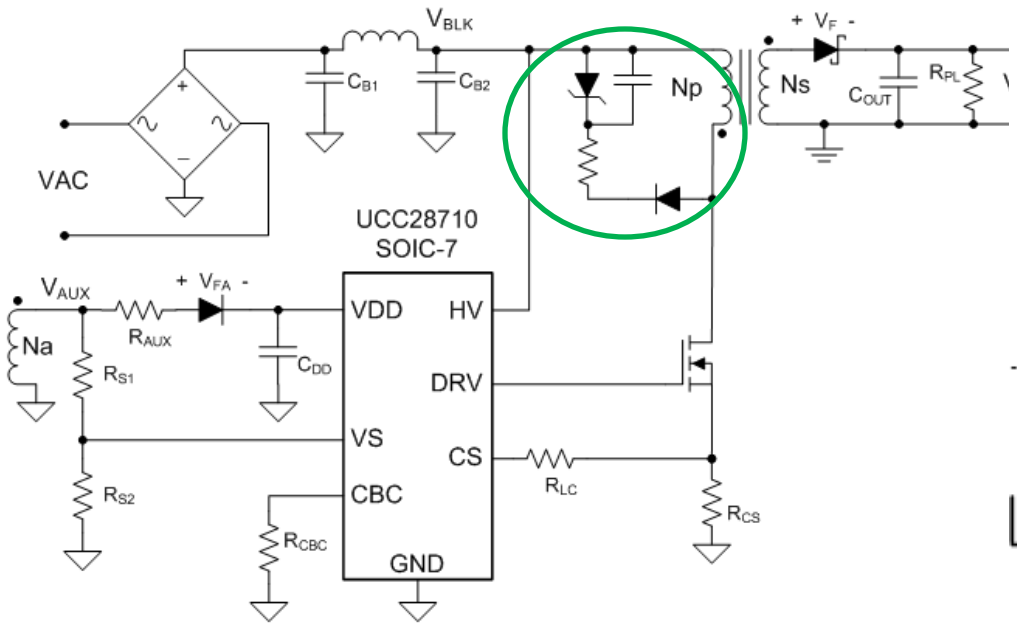
Design Tips and Recommendations

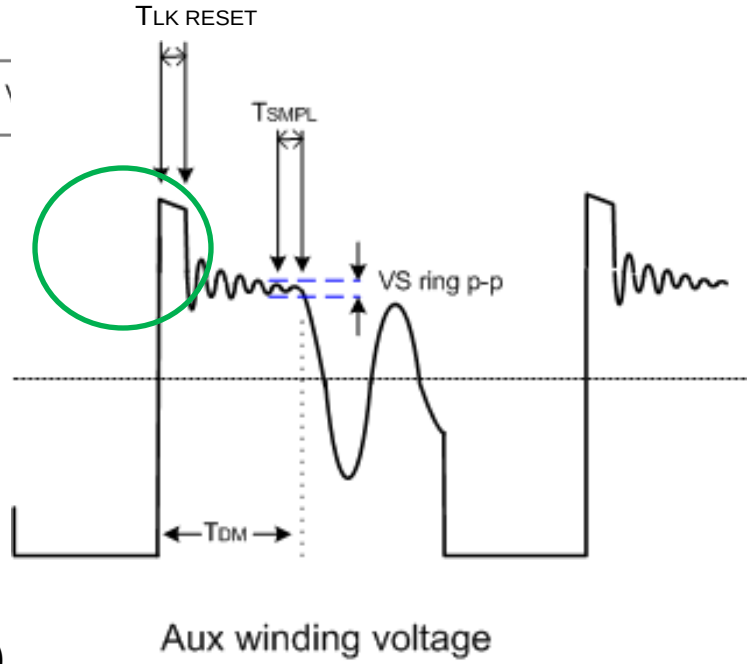
- ✓ Common Problems With PSR Flyback Designs
  - ✓ Excessive low frequency ripple on V_{OUT}, usually at lighter loads
    - ✓ Waveform on aux winding/VS pin: Result in no or incorrect V_{OUT} sensing
      - ✓ Too much ringing during all of Dmag time can result in no sample
      - ✓ Leakage reset pulse is too long, beyond blanking time, incorrect sample
      - ✓ Don't probe the VS pin directly with a scope probe, examine aux winding
  - ✓ V/I Curve: Voltage out of regulation before Constant Current limit
    - ✓ Converter reaches power limit before constant current limit at nominal V_{OUT}, usually at low V_{IN}
      - ✓ Transformer reaches transition mode limit at low line before P_{OUT} max
        - ✓ Increase turns ratio, or increase V_{BULK} min (larger cap)
      - ✓ Converter reaches F_{MAX} limit of IC
        - ✓ Increase transformer inductance to reduce Fsw

Design Tips and Recommendations

- ✓ Common Problems With PSR Flyback Designs
  - ✓ Standby (no load) power too high
    - ✓ The converter can not meet standby power target, and Fsw is close to IC minimum limit
      - ✓ Too much energy in IPP minimum pulse.
        - ✓ Too much Drain node capacitance
        - ✓ IPP min is too high
  - ✓ Vout regulation at no load, high line
    - ✓ Converter is running at Fswmin limit, cannot reduce V_{OUT}
      - ✓ V_{OUT} preload resistor is not low enough value
      - ✓ Too much energy in IPP minimum pulse.
        - ✓ Too much Drain node capacitance
        - ✓ IPP min is too high

Design Tips and Recommendations
V_{OUT} LF ripple, V_{AUX} waveform

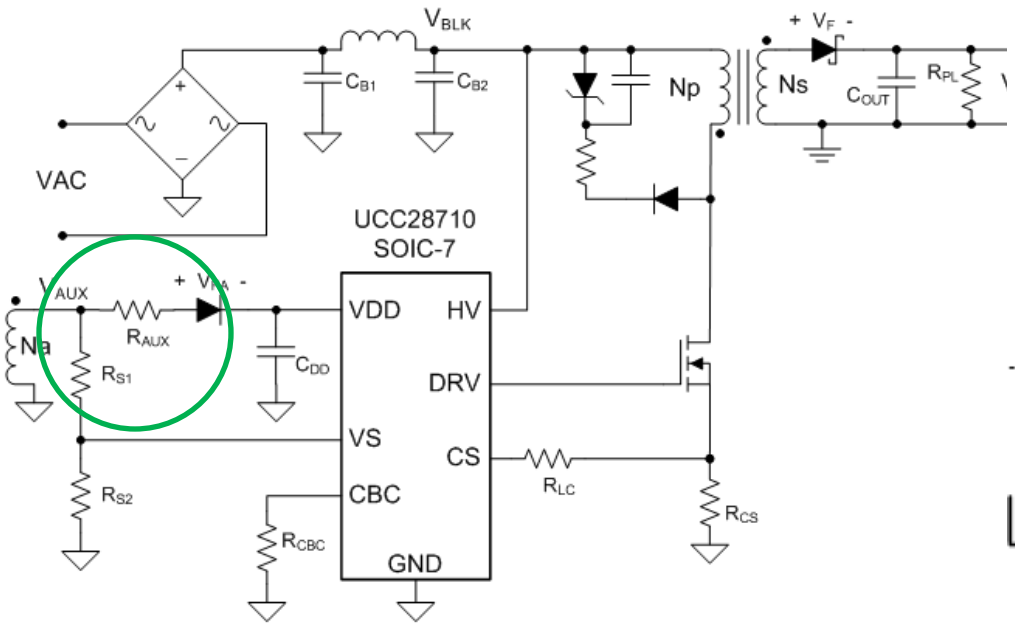


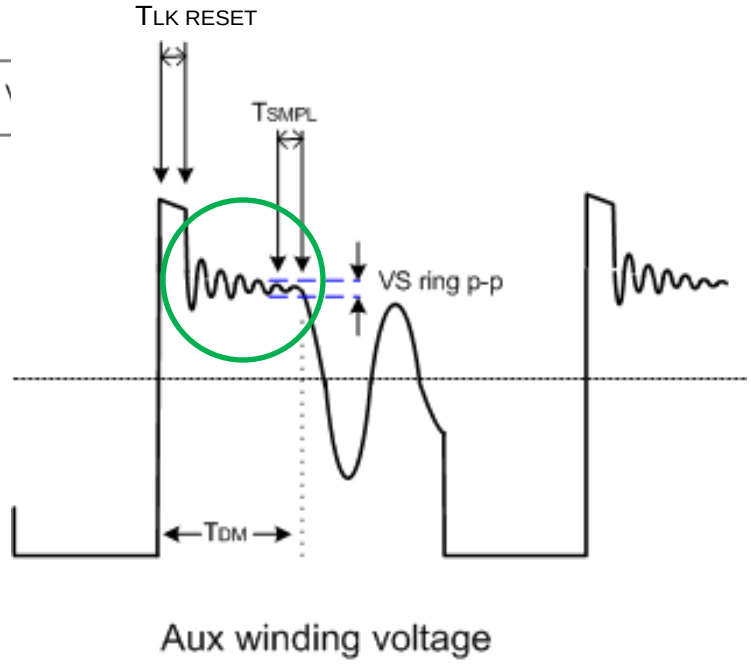


Aux winding voltage

- ✓ VS Signal Leakage Reset Spike (T_{LK_RESET})
  - ✓ Keep T1 Primary Leakage < 5%
  - ✓ T_{LK_RESET} < 2.4us @ I_{PP} Max
  - ✓ T_{LK_RESET} < 600ns @ I_{PP} Min
    - ✓ T_{LK_RESET} can be reduced by increased clamp voltage
    - ✓ Clamp diode recovery time will affect T_{LK_RESET}.
      - ✓ Look at fast aux diode (25-50ns) and 250 to 500ns clamp diode.

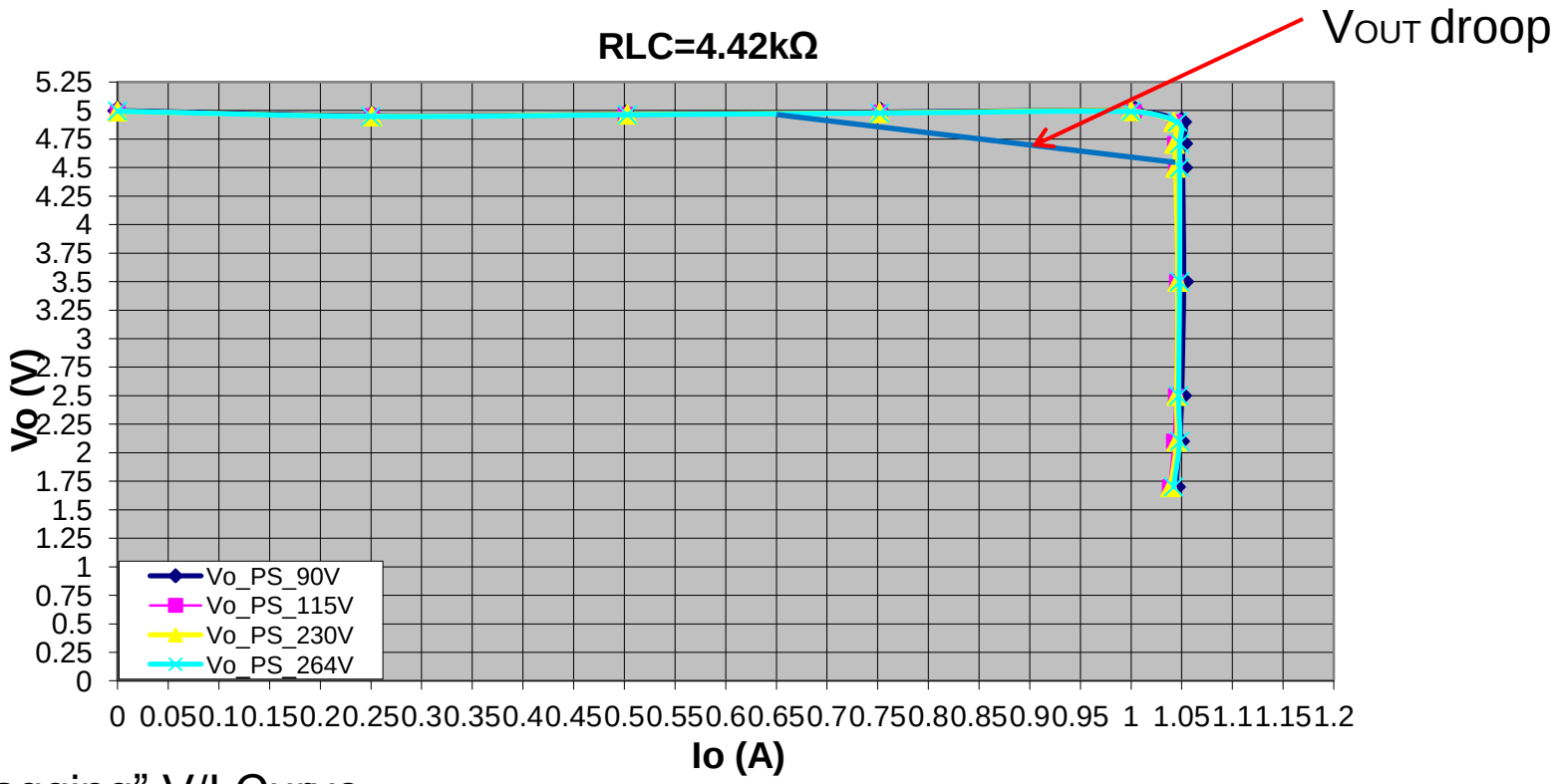
Design Tips and Recommendations
V_{OUT} LF ripple, V_{AUX} waveform





- ✓ VS Signal Leakage Induced Ringing (VS ring p-p)
  - ✓ Leakage spike induces ringing
  - ✓ Ringing on the VS pin needs to be <100mV p-p for at least 200ns before the knee
  - ✓ On Aux waveform ringing target is 100mV x (RS1+RS2)/RS2
    - ✓ Increase damping by increasing R_{AUX} value.

Design Tips and Recommendations
V/I Curve, V_{OUT} out of regulation before CC



- ✓ "Sagging" V/I Curve
  - ✓ If Vout drops before CC limit at low line only: transformer is at TM limit before max power at low line. Decrease Np/Ns, or increase input cap.
  - ✓ If Vout drops before CC limit at all line conditions: Fsw is reaching IC limit of 100kHz before full power. Increase primary inductance, lower Fsw.

Design Tips and Recommendations
Standby Power Too High: Dynamic Range

$$P_{in} = \frac{1}{2} I_{pk}{}^{2} L_p f_S$$

$$P_{in\_min} = \frac{1}{2} I_{pk\_min}{}^{2} L_p f_{S\_min}$$

$$P_{in\_max} = \frac{1}{2} I_{pk\_max}{}^{2} L_p f_{S\_max}$$

$$\frac{P_{in\_max}}{P_{in\_min}} = \left(\frac{I_{pk\_max}}{I_{pk\_min}}\right)^2 \frac{f_{S\_max}}{f_{S\_min}}$$

100kHz

680Hz

2350

4

-Must have reasonable expectations!
-Will not achieve 10mW at 15W Pout!
  <8mW achieved at 6W
  ~20mW achieved at 15W w/SR
-Keep total Drain node capacitance low
  -Transformer construction
  -MOSFET

6W design example at 230V AC

P_{in_min}	IC	Snubber	Coss (50pF) associated loss	Total
2.6mW	2.0mW	.5mW	3.5mW	8.1mW

Wide control dynamic range achieves low stand by power

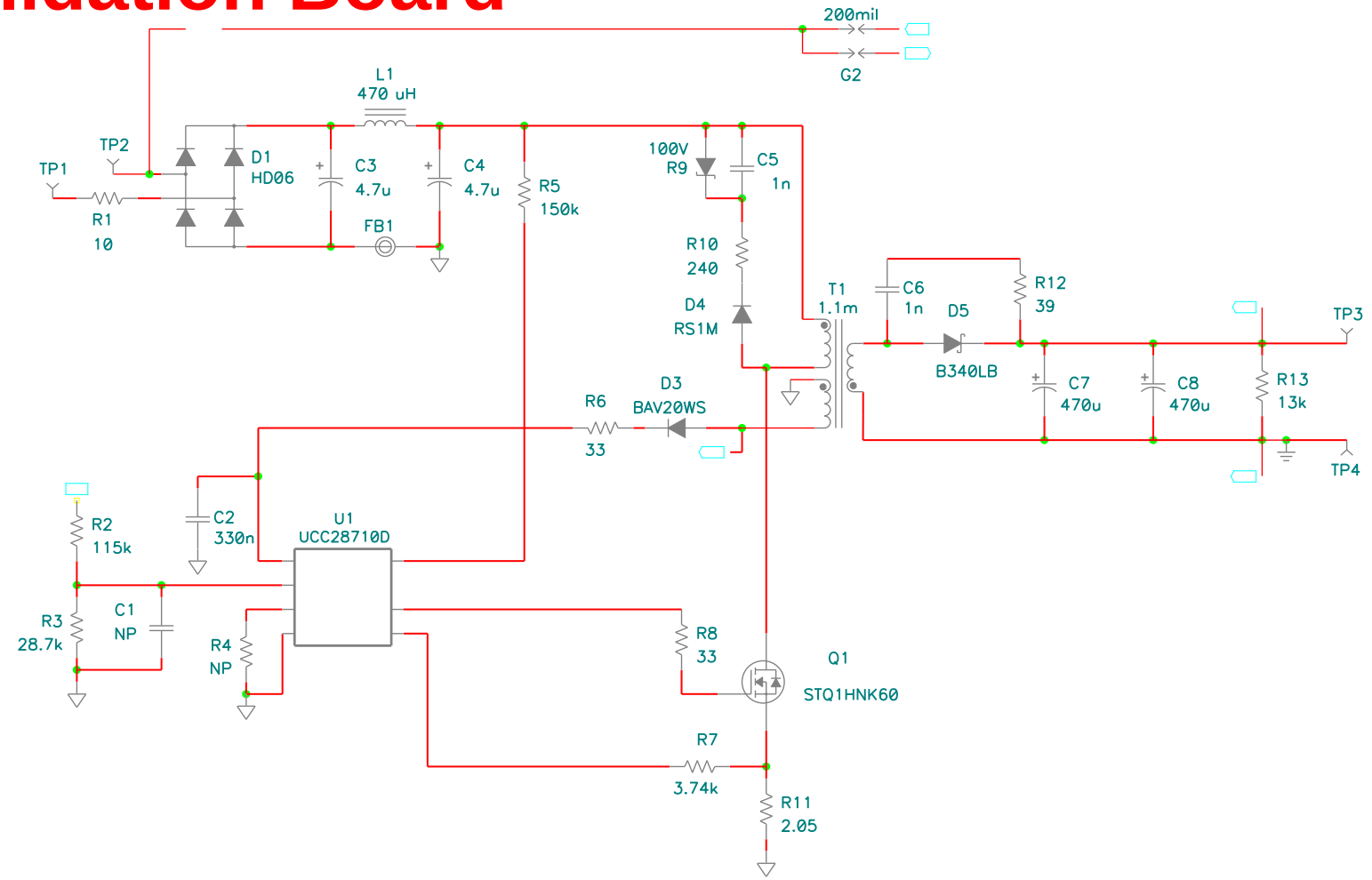
TI Low Power Flyback Solutions

	PSR	HV Start	Device	NTC	CBC
UCC2870X	Yes	No	MOSFET	Option	Option
UCC2871X	Yes	Yes	MOSFET	Option	Option
UCC28720	Yes	Yes	BJT	Yes	No
UCC28722	Yes	No	BJT	Yes	No
UCC28740	No	Yes	MOSFET	No	No
UCC28910	Yes	Yes	Integrated MOSFET	Yes	No

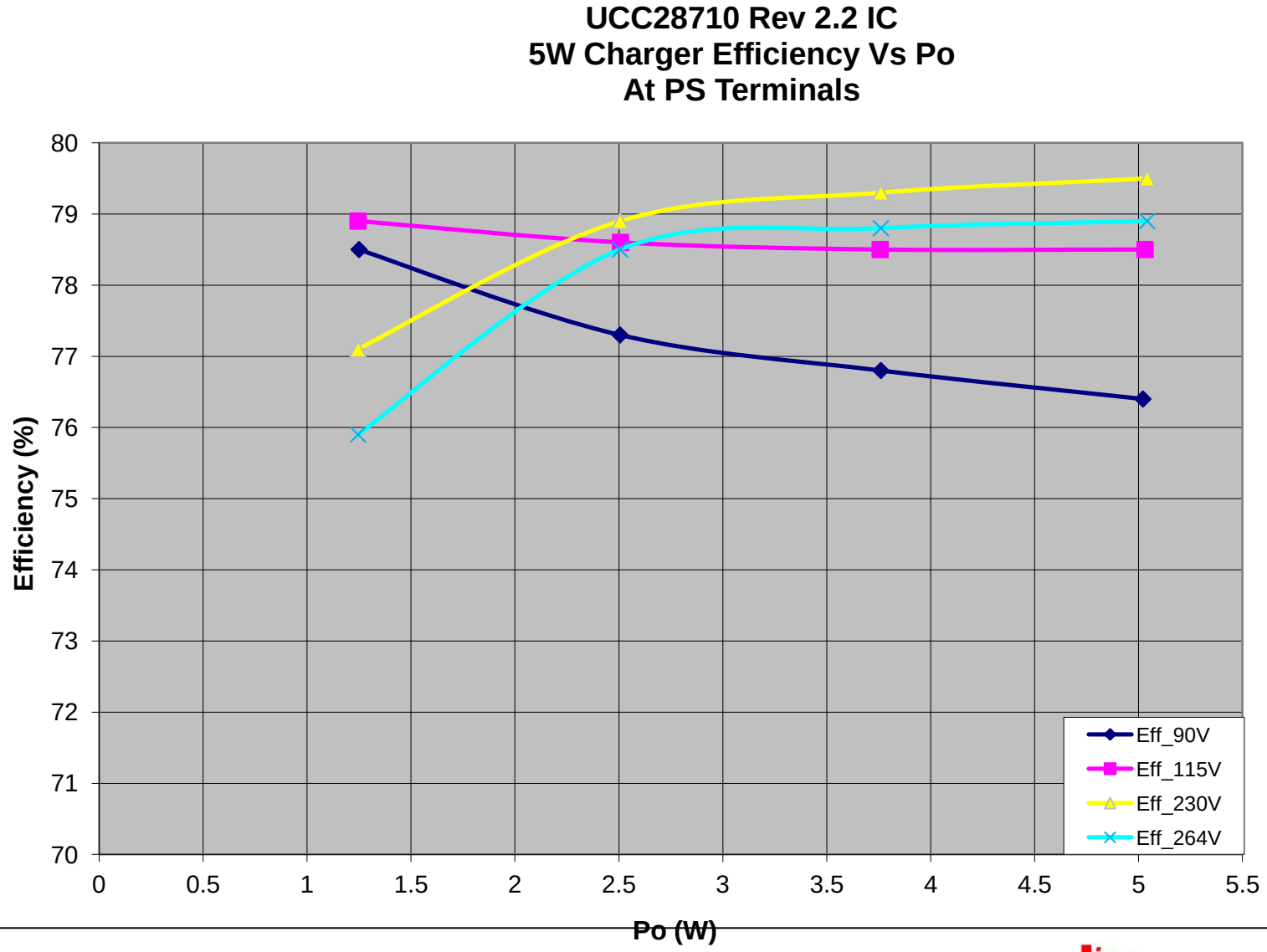
- TI provides varies solutions targeting for low power AC/DC adapters
- Solutions with primary and secondary side regulation
- MOSFET and BJT driving capability
- Minimize cost and standby power

THANKS!

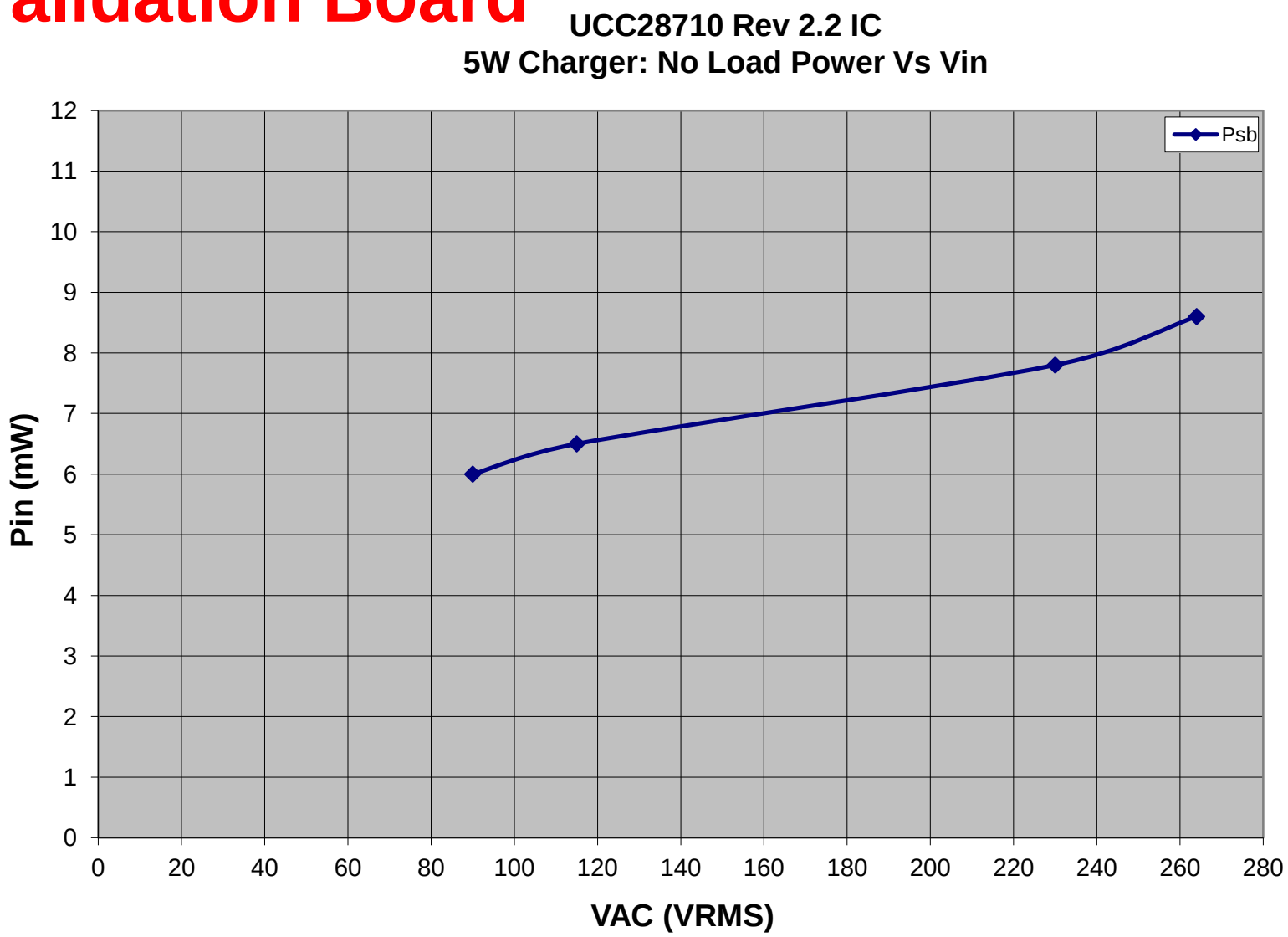
5.5 W UCC28710 Schematic Validation Board



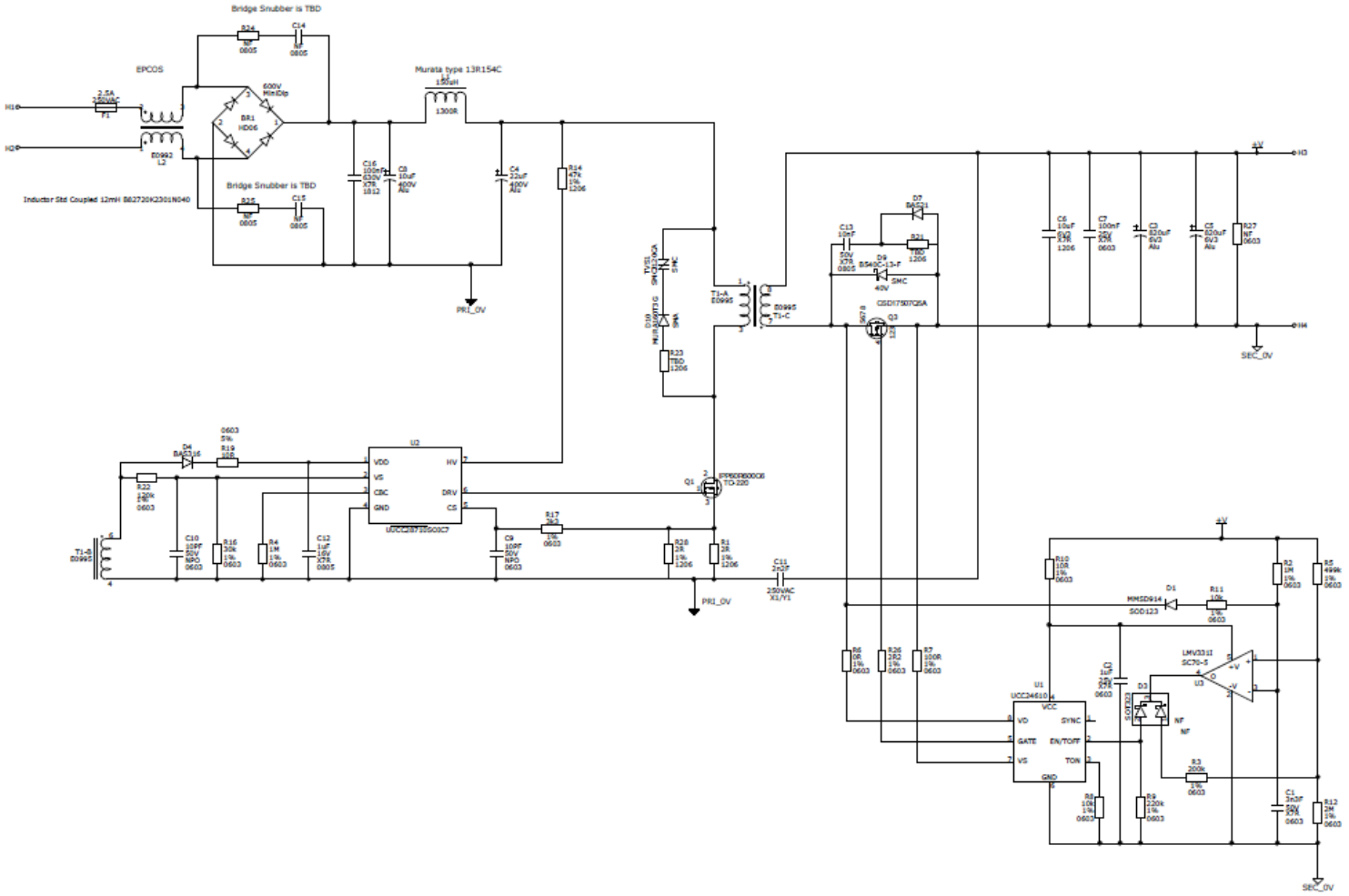
5.5 W UCC28710 Efficiency Validation Board



5.5 W UCC28710 No Load Power Validation Board



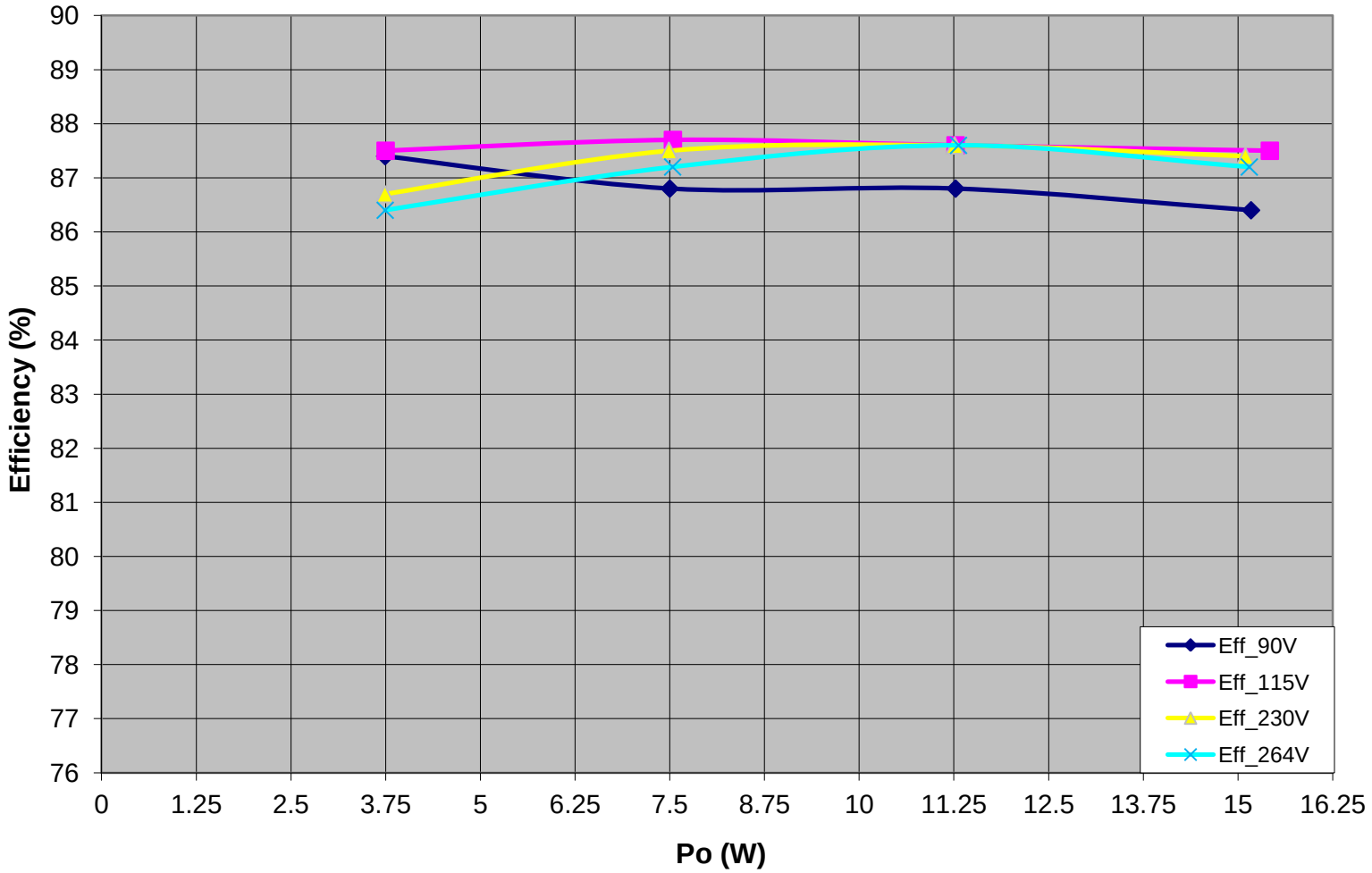
15 W UCC28710/UCC24610 Schematic APEC Demo



15 W UCC28710/UCC24610 Efficiency APEC Demo

UCC28710/UCC24610
15W Charger: Efficiency Vs Po
At PS Terminals

Average Efficiency
115V: 87.6%
230V: 87.3%



15 W UCC28710/UCC24610 No Load Power APEC Demo