New Times are Coming –
Digitally Operated Primary Control Technology for AC/DC SMPS

Abstract

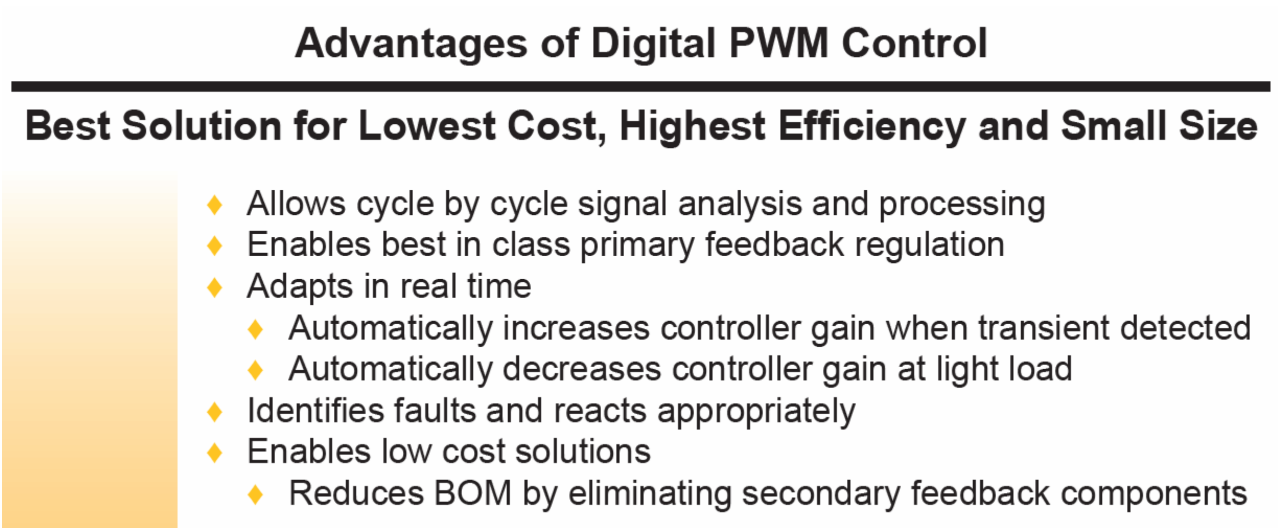
This paper describes a whole new control technique and had been successfully being employed in off-line type adapter/charger applications, which results in significant reduction to external components and various performance improvements.

Introduction

A new digital control methodology has resulted in greater simplicity and design flexibility in low power SMPS topologies which conventional analog methods would find difficult if not impossible to achieve. By combining this new control scheme into an off-line type of adapter or charger application, it could greatly reduce the number of external components as well as enhance supply performance in many respects.

The controller has built-in digital control algorithms to quickly and smoothly transition between different operating modes for reduced switching losses during no-load operation. The full-load efficiency is enhanced by the use of so-called “emulated primary current mode control” to eliminate the need for a primary sensing resistor. The full-load efficiency is also enhanced in cellular charger applications by the elimination of secondary-side constant current sense circuitry. Its unique digital control algorithm allows fast pulse-by-pulse analysis of the switching waveform and provides accurate voltage & constant-current regulation from the primary-side without the need for an opto-coupler, secondary feedback and reference circuits required by traditional analog solutions.

This innovative technology is ideal for balancing new regulatory requirements for green-mode operation with more practical design considerations such as lowest possible cost, smallest size and highest efficiency.



Digital PWM Operation

Three modes of operation are used to generate the CV/CC curve as shown in Figure 1. The digital control algorithm was optimized to provide all of the required operating modes with stable transitions between modes. The controller operates in PWM mode during higher output power levels and switches to PFM mode at light load to minimize power dissipation. The details of the method of operation of each of the modes are given below.

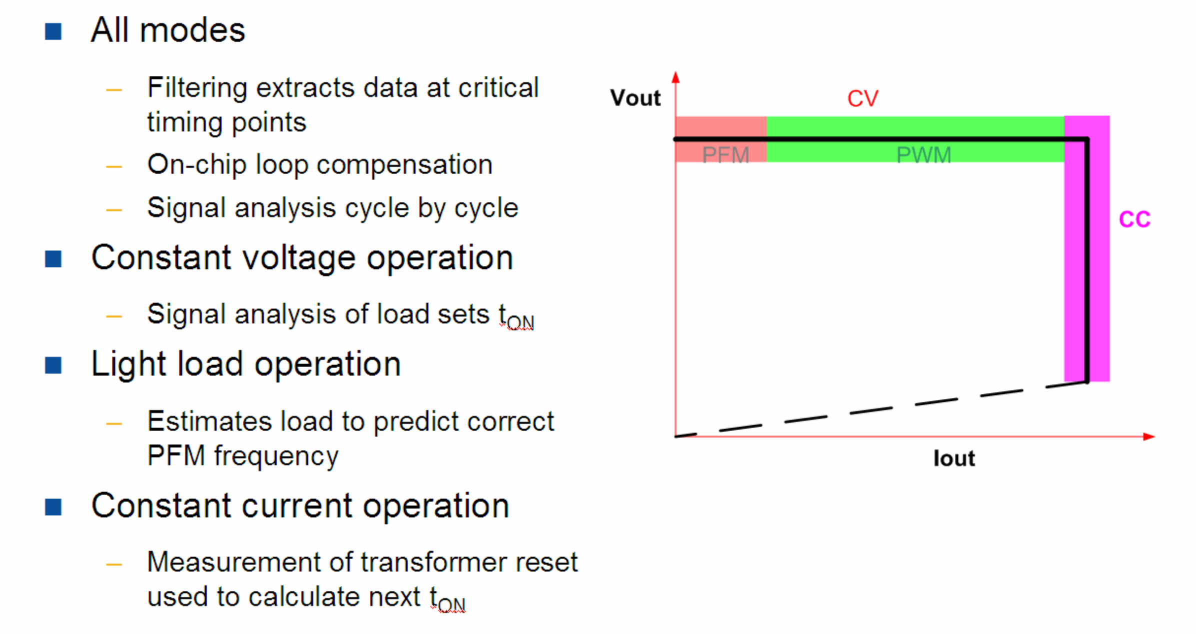


Figure-1, Modes of Operation

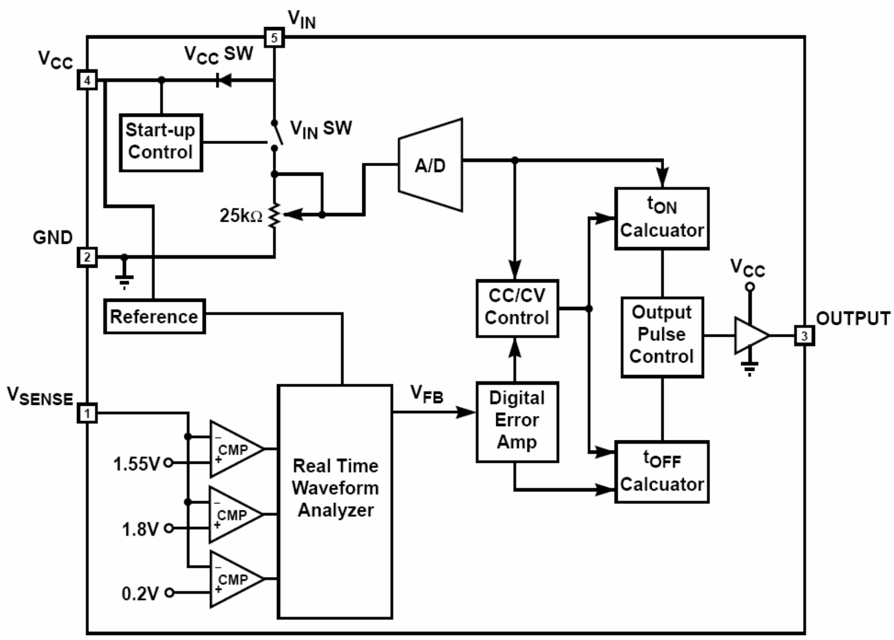
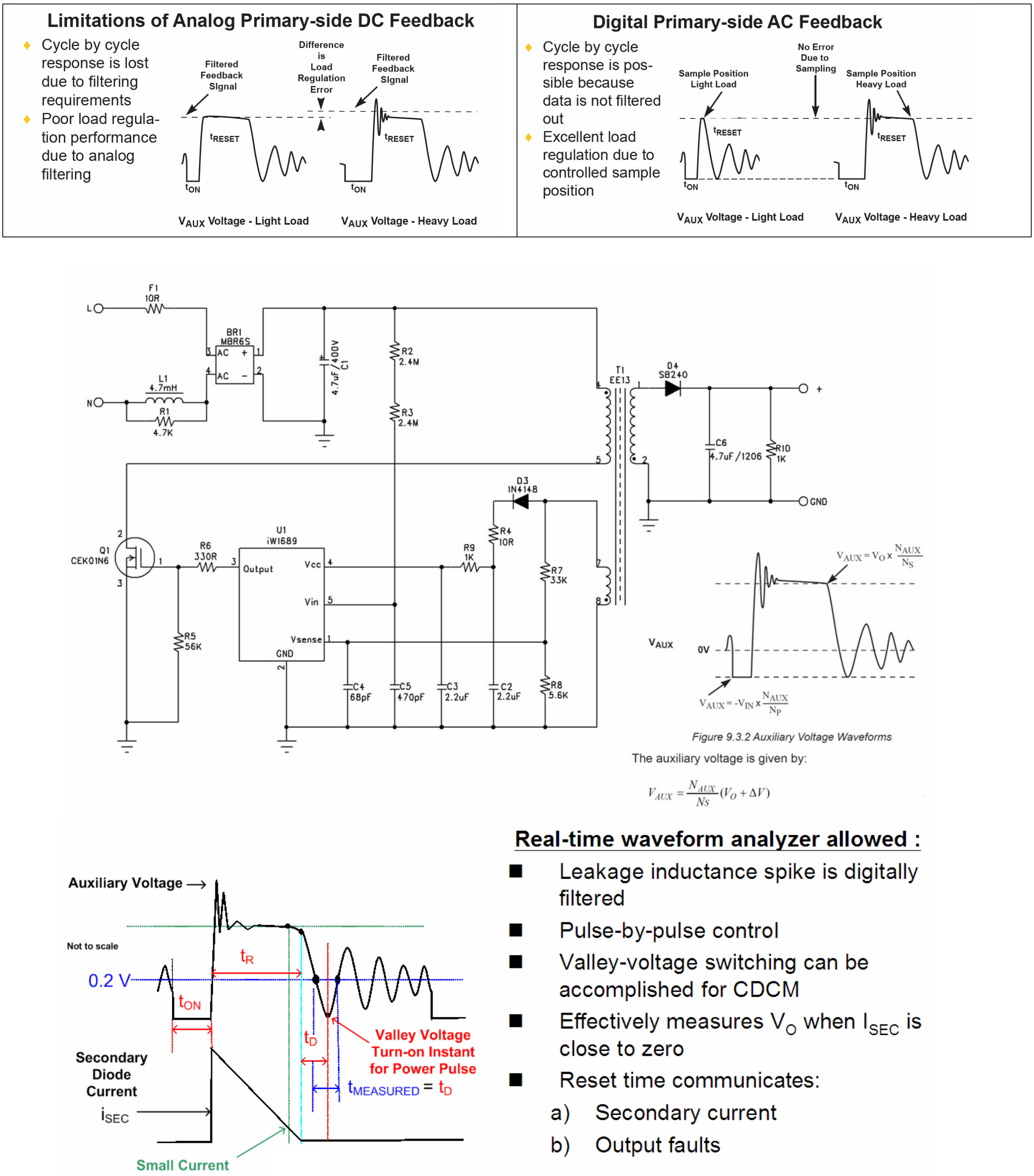


Figure-2, Digital PWM Controller Functional Block Diagram

1. **Constant Voltage Operation**

Output voltage regulation is accomplished by a primary-side control technique and eliminates the need for the Opto-coupler feedback and secondary voltage reference found in traditional designs. The state of the output is derived by the digital algorithm's analysis of each and every primary auxiliary winding waveform in "real-time" and is then fed into the Digital Error Amplifier (DEA) to generate a PWM output for switching. This technique yields accurate voltage regulation of better than ±1.5% under all possible line and load conditions. The superiority of the performance as compared to traditional primary feedback solutions is further detailed in Figure 3.



$$V_{AUX} = V_O \times \frac{N_{AUX}}{N_S}$$

$$V_{AUX} = -V_{IN} \times \frac{N_{AUX}}{N_P}$$

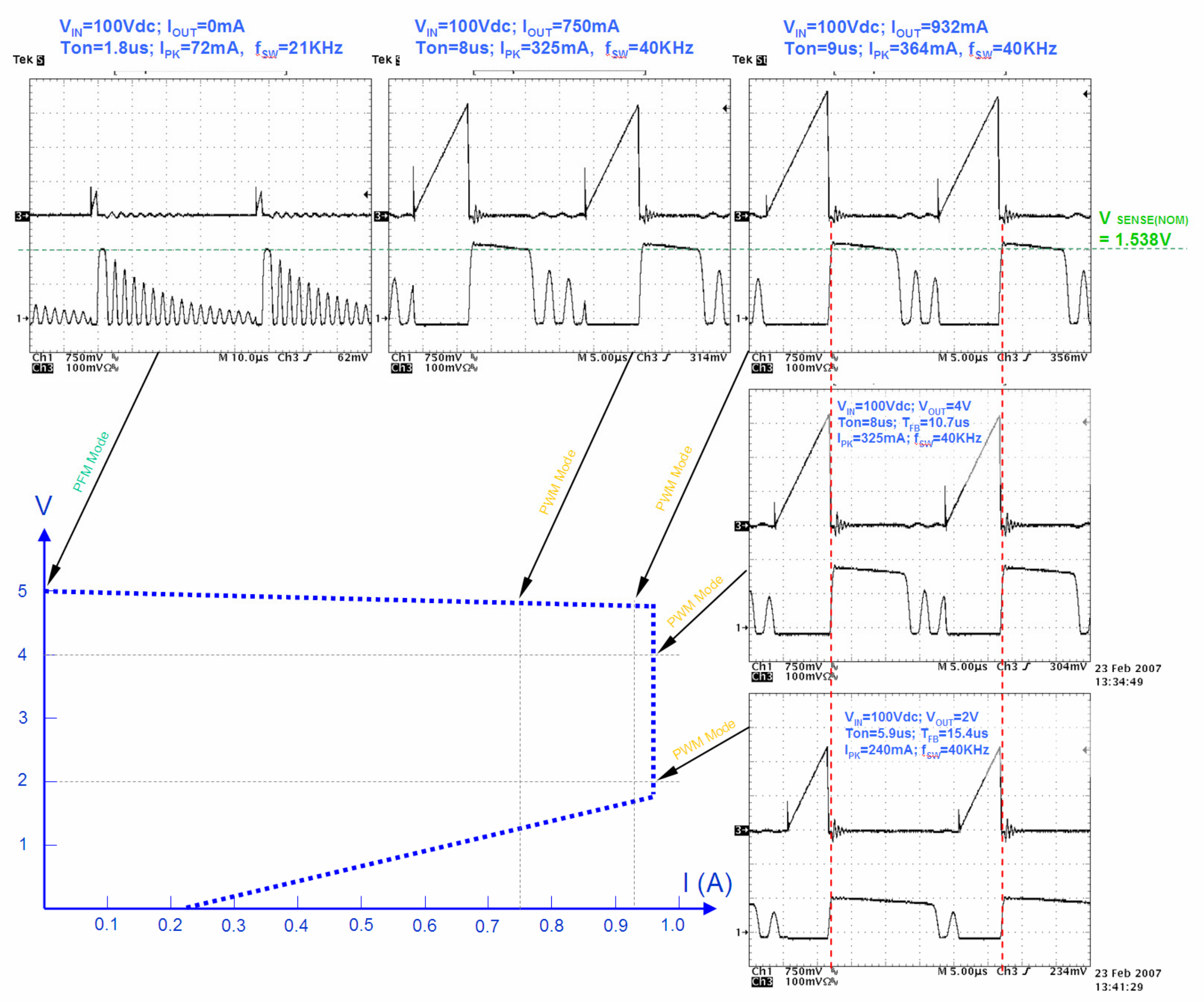
$$V_{AUX} = \frac{N_{AUX}}{N_S}(V_O + \Delta V)$$

Figure-3, Primary-Side Regulation

2. Constant Current Operation:

The constant current (CC) feature uses the same feedback technique as in constant-voltage mode, but monitors both the line voltage and the output voltage feedback signal. These signals are processed and passed on to the DEA and t_{ON}/t_{OFF} calculator blocks. The accuracy of this control technique yields superior CC tolerance (typically ±2%) excluding the tolerance of the transformer's primary inductance.

This combination of control techniques allows the designer to eliminate all secondary current and voltage sensing circuitry, resulting in a simple, low cost solution with improved efficiency.



$$I_O = \frac{V_g \times t_{on} \times N \times t_R}{2 \times L_M \times T_S} = \left(\frac{V_g \times t_{on}}{2 \times L_M} \times N \times \frac{1}{T_S}\right) \times t_R$$

The tolerance of Lm can be corrected by trimming the input voltage (Pin5).

$$V_g = V_{IN\_PIN5} \times \frac{R_{IN} + 0.02}{0.02}$$

$$t_{on} = \frac{K}{t_R \times V_g}$$

Figure-4, Constant Current Operation

3. **Protection Features (Primary UV, OV, Secondary OVP, OCP & SSP):**

   a. <u>Primary Overvoltage & Undervoltage Protection</u> is provided by monitoring the V_{IN} voltage (also the bulk-cap voltage) to shut down the switching operation when the threshold is exceeded for more than a specified number of cycles.

   b. <u>Secondary Overvoltage Protection</u> is accomplished by monitoring the V_{SENSE} pin threshold. The IC will shut down after a specified number of consecutive fault condition switching pulses. The IC will then attempt to restart.

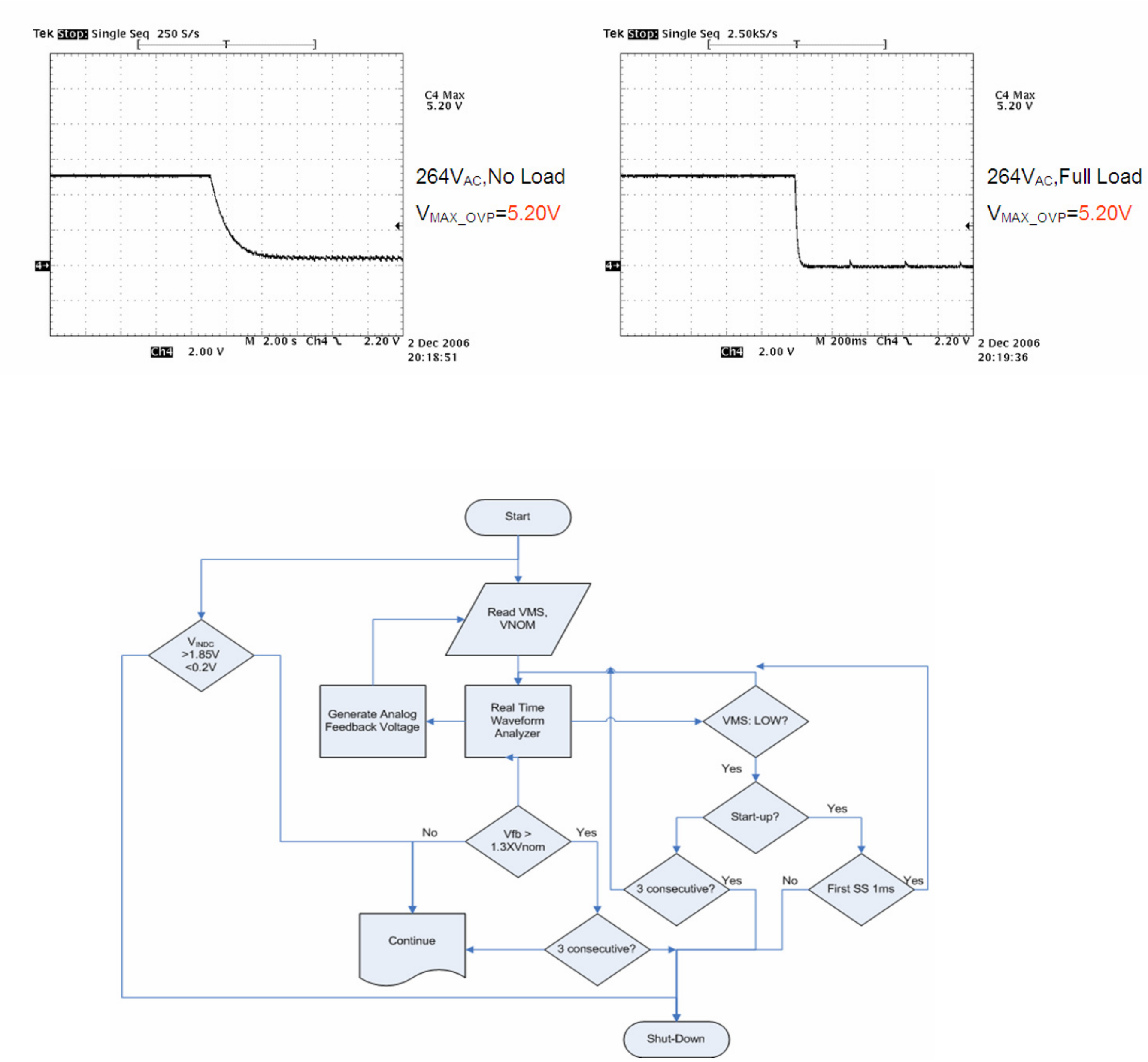


Figure-5, Overvoltage Shutdown Waveforms & Decision Tree

c. <u>Secondary Over Current Protection (applied to adapter with single output design)</u> limits the output current to within a small range independent of AC input line voltage variations.

$$P_{O\_MAX} = \frac{(V_g \times t_{on})^2}{2 \times L_M \times T_S} \times \eta$$

$$\Rightarrow I_{OCP} = \frac{(V_g \times t_{on})^2}{2 \times L_M \times T_S \times V_{OUT}} \times \eta$$

Note:

$(V_g \times t_{on})$: Constant Parameter(= 900V · us)

L_M : Coupling Inductance Between Primary and Secondary

T_S : Operational Period Time

η : Efficiency (Except Primary - Loss)

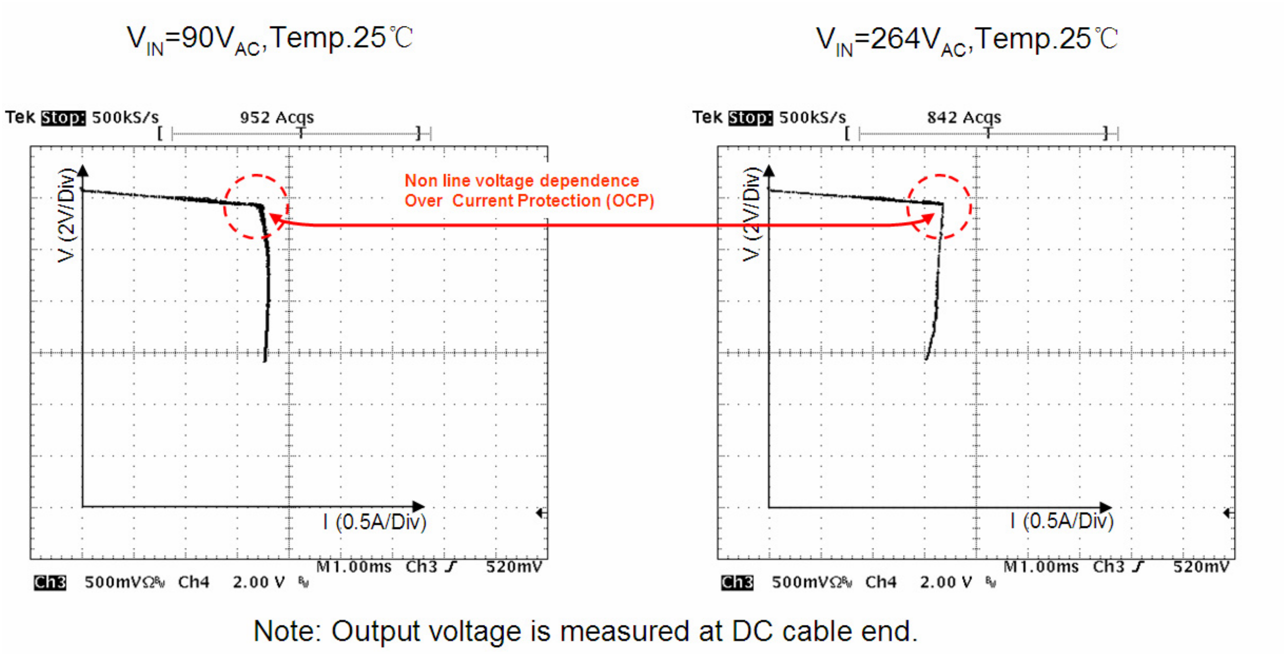


Figure-6, Secondary Over-Current Protection

d. Secondary Output Short-circuit Protection is provided through analysis of the primary V_{SENSE} waveform obtained from the bias winding and is based on a scheme to avoid core saturation.

1. Ensures each cycle is fully reset before next on pulses is applied.
2. Limits operating V-s (1050V-μs) to guarantee V_{MAX} will not be exceeded in a given switching cycle.

This technique ensures that no buildup of flux energy in the core can occur from cycle to cycle. To avoid operation in continuous conduction (CCM) mode, the controller checks for the falling edge of the V_{SENSE} input on every cycle. If a falling edge of V_{SENSE} is not detected during the normal 25 μs period, the switching period will be extended until the falling edge V_{SENSE} does occur. If the switching period reaches 75 μs without V_{SENSE} being detected, the controller will immediately shut off.

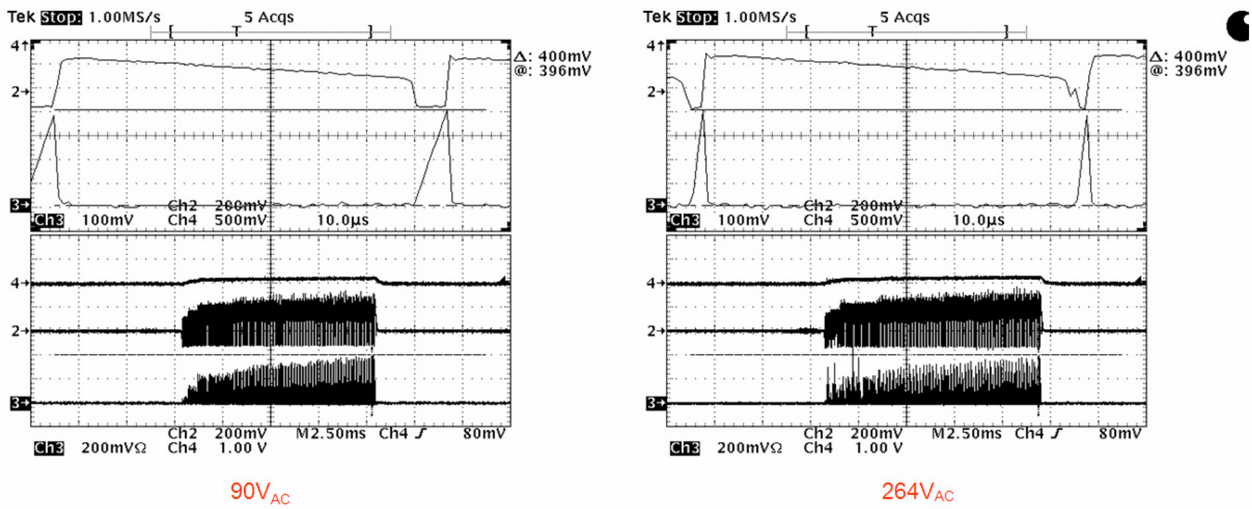
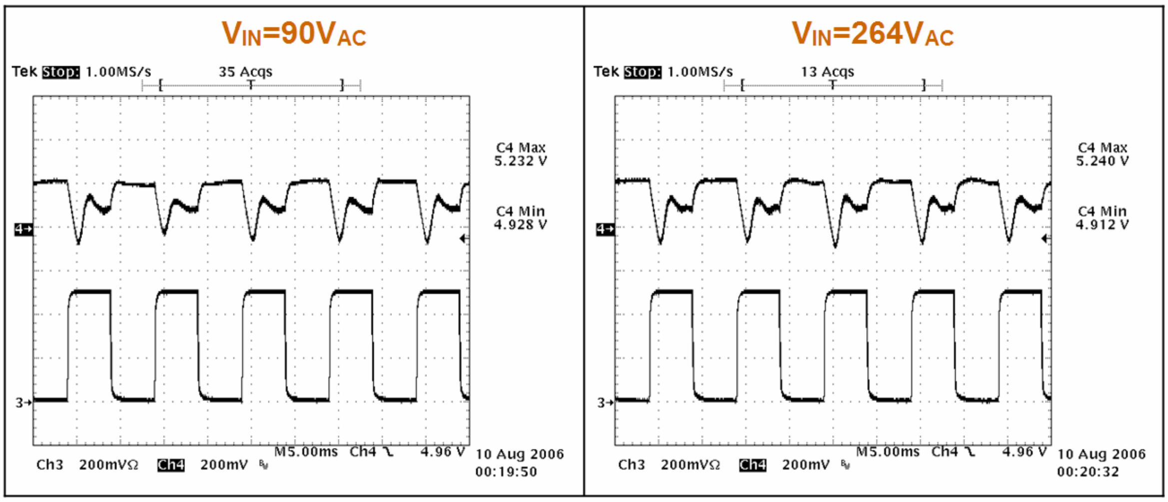


Figure-7, Output Short Circuit Protection

Other Features :

1. Dynamic Response is improved by adjusting to the control loop gains based on the amount of deviation from a reference. The loop gain is increased by four times when the IC sees a significant load change and reduces the gain back when load conditions stabilize.



Note: Step Load 0A-0.5A-0A; Slew rate: 0.1A/us

2. <u>Soft-Start</u>

The device incorporates an internal soft-start function with no external components. The soft-start time is set at 3.5 ms. Once the V_{IN} pin voltage has reached its turn-on threshold, the controller starts switching, but limits the ON-time to a percentage of the maximum ON-time as shown in Figure 9. If the output voltage rises above the minimum threshold before soft-start is completed, the device assumes that the output load is very light and immediately changes to PFM operation.

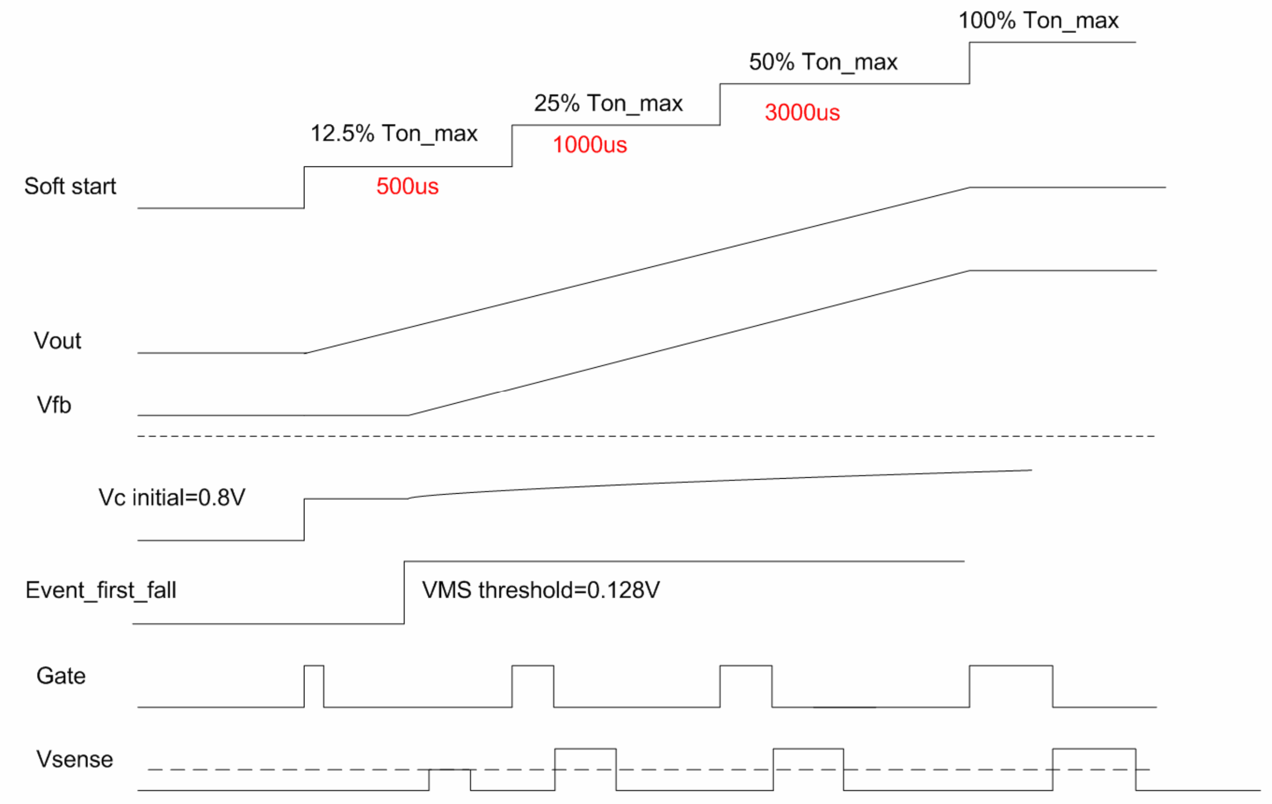


Figure-8, Soft Start

Conclusion :

iWatt's digital control scheme is specifically designed to address the challenges and trade-offs of low power adapters and chargers. This innovative technology is ideal for balancing new regulatory requirements for green mode operation with more practical design considerations such as lowest possible cost, smallest size and high performance output control. It is unique compared to traditional analog controllers in that it can provide secondary-side performance while utilizing the more cost-effective primary-side control techniques.

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