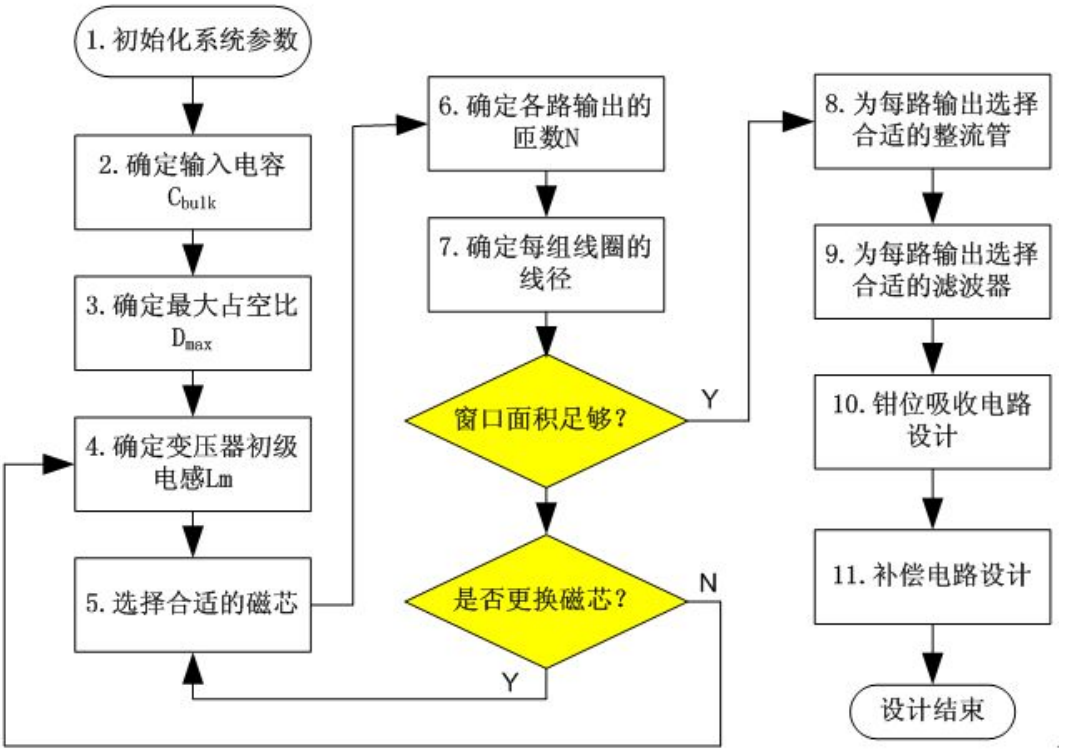
Flyback Converter Design

Prepare by：Carey Hu

Engineering and Technical Support Center

2014.02.28

This document aims at presenting a guidelines for designing flyback converter, and the overal procedures is as below.



Now,we will start the designing step-by-step as above in details..

Step1:初始化系统参数

（*Initial the systerm parameters*）

------输入交流范围：　$V_{inmin\_AC} := 90V$　　$V_{inmax\_AC} := 265V$

------电网工频：　$f_{line} := 50Hz$

------输出：

$V_{out1} := 5V$ $I_{out1} := 1A$

$V_{out2} := 15V$ $I_{out2} := 0.1A$

$P_O := V_{out1} \cdot I_{out1} + V_{out2} \cdot I_{out2} = 6.5\,W$

------开关频率：

$f_{sw} := 100kHz$

------预估效率：

$\eta := 0.8$

$$P_{in} := \frac{P_O}{\eta} = 8.125\,W$$

------各路输出功率占比：

$$K_{L1} := \frac{V_{out1} \cdot I_{out1}}{P_O} = 0.769$$

$$K_{L2} := \frac{V_{out2} \cdot I_{out2}}{P_O} = 0.231$$

Step2:确定输入电容Cbulk

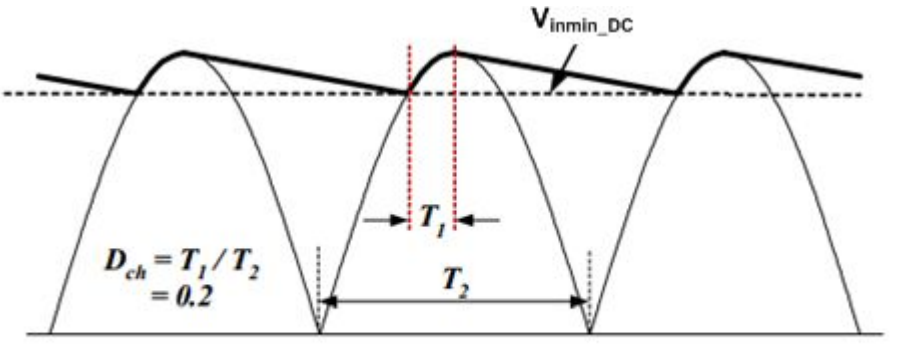
（Determine the input capacitor Cbulk）

------宽压输入，3μF/W，取15μF+14.7μF两个400V高压电容并联：

$C_{bulk} := 19.7\mu F$

------计算整流后最小直流电压：

$D_{ch} := 0.2$



每个周期只有T1时间段内，电网对Cbulk电容充电

$$V_{inmin\_DC} := \sqrt{\left(\sqrt{2}\cdot V_{inmin\_AC}\right)^2 - \frac{P_{in}\cdot\left(1 - D_{ch}\right)}{C_{bulk}\cdot f_{line}}} = 97.985\,V$$

Step3:确定最大占空比Dmax
（Determine the Dmax）

------NCP1015工作于DCM模式，最大占空比取：

$$D_{max} := 0.45$$

------计算反射电压：

$$V_{or} := \frac{D_{max}}{1 - D_{max}}\cdot V_{inmin\_DC} = 80.169\,V$$

Step4:确定变压器初级电感Lm
（Caculate Primary inductance Lm of the transformer）

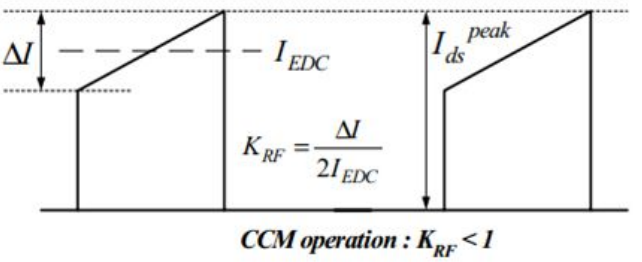
------DCM模式电流纹波系数：

$$K_{RF} := 1$$

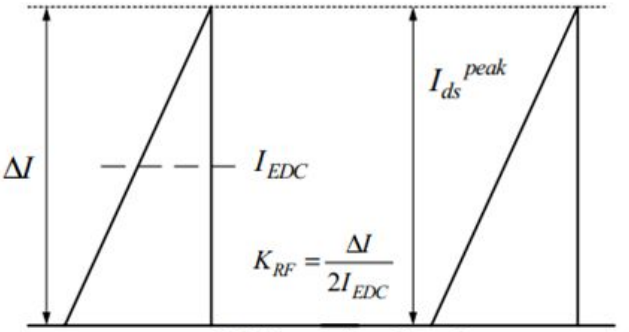
------计算初级电感：

$$L_m := \frac{\left(V_{inmin\_DC}\cdot D_{max}\right)^2}{2\cdot P_{in}\cdot f_{sw}\cdot K_{RF}} = 1.196\times 10^{-3}\,H$$

------计算初级电流峰值：



CCM operation : $K_{RF}<1$



DCM operation : $K_{RF}=1$

$$I_{EDC} := \frac{P_{in}}{V_{inmin\_DC} \cdot D_{max}} = 0.184A$$

$$\Delta I := \frac{V_{inmin\_DC} \cdot D_{max}}{f_{sw} \cdot L_m} = 0.369A$$

$$I_{dspeak} := I_{EDC} + \frac{\Delta I}{2} = 0.369A$$

------计算初级电流RMS：

$$I_{dsrms} := \sqrt{\left[3 \cdot I_{EDC}^{2} + \left(\frac{\Delta I}{2}\right)^{2}\right] \cdot \frac{D_{max}}{3}} = 0.143A$$

------计算MOS的导通损耗，NCP1015内置MOS的Rdson为11Ω：

$$R_{dson} := 11\Omega$$

$$P_{cond} := I_{dsrms}^{2} \cdot R_{dson} = 0.224W$$

Step5:选择合适的磁芯，计算初级电感Lm匝数
（Select proper core ，caculate primary Lm turns Np）

------磁芯选择EFD20，根据磁芯手册可知：

$$A_e := 31mm^2$$

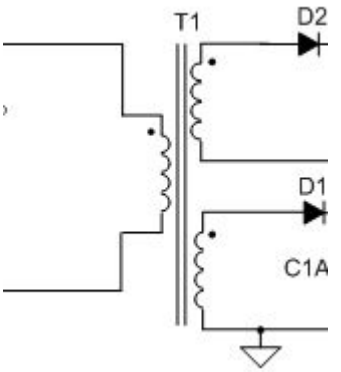
------DCM模式，磁通摆幅：

$$\Delta B := 0.21T$$

------初级电感匝数：

$$N_p := round\left(\frac{L_m \cdot I_{dspeak}}{\Delta B \cdot A_e}\right) = 68$$

Step6:确定各路输出的匝数
（Determine the turns of each output）



设各路输出整流管的正向导通压降相同：

$$V_F := 0.5V$$

------主路：

$$N_{s1} := round\left(\frac{V_{out1} + V_F}{V_{or}} \cdot N_p\right) = 5$$

------辅路：

$$N_{s2} := round\left(\frac{V_{out2} + V_F}{V_{out1} + V_F} \cdot N_{s1}\right) = 14$$

------IC供电辅助线圈：

$$V_{aux} := 20V$$

$$N_a := round\left(\frac{V_{aux} + V_F}{V_{out1} + V_F} \cdot N_{s1}\right) = 19$$

Step7:确定每个绕组的线径

（Determine the wire demission for each output）

根据流过每个绕组电流的RMS决定导线线径，导线电流密度取：

$$\rho := 8\,\frac{A}{mm^2}$$

------初级Lm：

$$I_{prms} := I_{dsrms}$$

$$D_p := 2 \cdot \sqrt{\frac{I_{prms}}{\rho \cdot \pi}} = 0.151 \cdot mm$$

------次级主路：

$$I_{secrms1} := I_{dsrms} \cdot \sqrt{\frac{1 - D_{max}}{D_{max}}} \cdot \frac{V_{or} \cdot K_{L1}}{V_{out1} + V_F} = 1.769\,A$$

$$D_{s1} := 2 \cdot \sqrt{\frac{I_{secrms1}}{\rho \cdot \pi}} = 0.531 \cdot mm$$

------次级辅路：

$$I_{secrms2} := I_{dsrms} \cdot \sqrt{\frac{1 - D_{max}}{D_{max}}} \cdot \frac{V_{or} \cdot K_{L2}}{V_{out2} + V_F} = 0.188\,A$$

$$D_{s2} := 2 \cdot \sqrt{\frac{I_{secrms2}}{\rho \cdot \pi}} = 0.173 \cdot mm$$

Step8:为每一路输出选择合适的整流二极管

（Select proper rectifier diode for each output）

------主路：

$$V_{D1} := V_{out1} + \frac{\sqrt{2}\cdot V_{inmax\_AC}}{V_{or}}\cdot\left(V_{out1} + V_F\right) = 30.711\,V$$

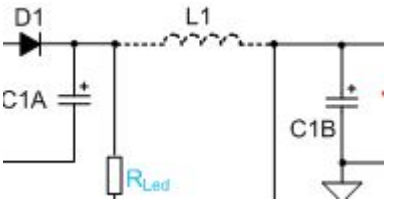
$$I_{Drms1} := I_{dsrms}\cdot\sqrt{\frac{1 - D_{max}}{D_{max}}}\cdot\frac{V_{or}\cdot K_{L1}}{V_{out1} + V_F} = 1.769\,A$$

------辅路：

$$V_{D2} := V_{out2} + \frac{\sqrt{2}\cdot V_{inmax\_AC}}{V_{or}}\cdot\left(V_{out2} + V_F\right) = 87.458\,V$$

$$I_{Drms2} := I_{dsrms}\cdot\sqrt{\frac{1 - D_{max}}{D_{max}}}\cdot\frac{V_{or}\cdot K_{L2}}{V_{out2} + V_F} = 0.188\,A$$

Step9:为每一路输出选择合适的滤波器
（Select proper filter for each output）



------主路：

输出电容Cout1承受的纹波电流为：

$$I_{caprms1} := \sqrt{I_{Drms1}^{\ 2} - I_{out1}^{\ 2}} = 1.46\,A$$

可选择两个470μF（16V）的Rubycon电容组成CLC滤波器，L取1μH

Rated capacitance (μF)	Size φD×L(mm)	Rated ripple current (mA r.m.s./105℃, 100kHz)	(Ω MAX) Impedance	
			20℃, 100kHz	−10℃, 100kHz
470	8×11.5	945	0.056	0.19

$$C_{out1} := 940\mu F \qquad Esr1 := \frac{0.056}{2}\Omega$$

则输出电压纹波为：

$$\Delta V_{out1} := \frac{I_{out1} \cdot D_{max}}{C_{out1} \cdot f_{sw}} + \frac{I_{dspeak} \cdot V_{or} \cdot Esr1 \cdot K_{L1}}{V_{out1} + V_F} = 0.12\,V$$

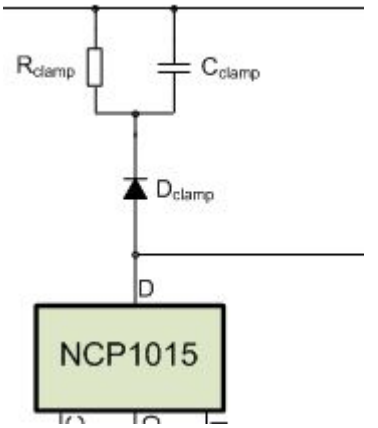
------辅路：

输出电容Cout2承受的纹波电流为：

$$I_{caprms2} := \sqrt{I_{Drms2}^{2} - I_{out2}^{2}} = 0.16\,A$$

Step10:钳位吸收电路设计

（*Clamp and snubber circuit design*）



------二极管Dclamp：

20W以下输出功率，钳位二极管采用1N4007即可：

------Rclamp：

$$V_{clamp} := V_{or} + 70V$$

$$L_{LK} := 0.05 \cdot L_m$$

$$R_{clamp} := 2 \cdot \frac{V_{clamp} \cdot \left(V_{clamp} - V_{or}\right)}{L_{LK} \cdot f_{sw} \cdot I_{dspeak}^{2}} = 25.875 \cdot k\Omega$$

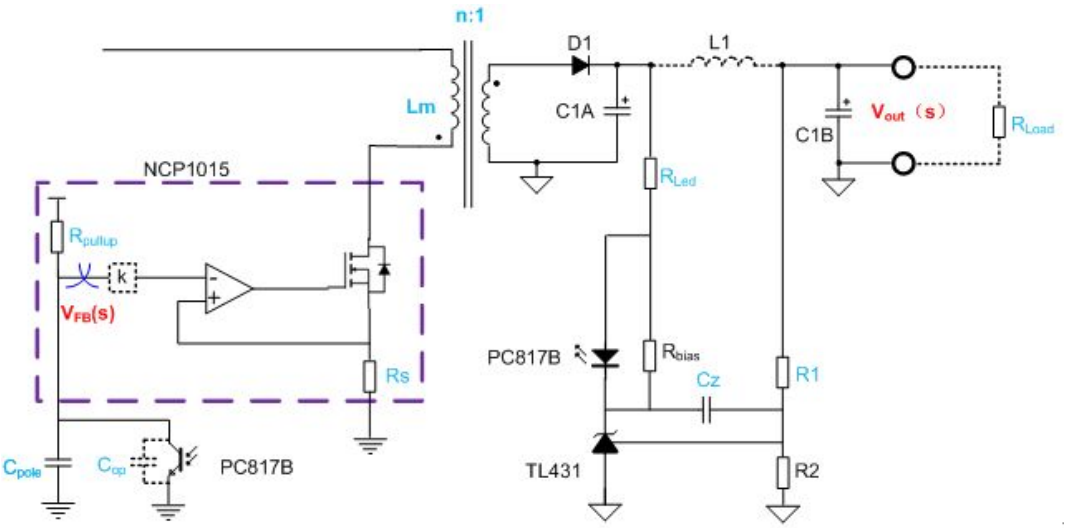
------Cclamp：

$$V_{ripple} := 0.1 V_{clamp}$$

$$C_{clamp} := \frac{V_{clamp}}{V_{ripple} \cdot f_{sw} \cdot R_{clamp}} = 3.865 \cdot nF$$

Step11:补偿电路设计

（Compensation circuit Design）

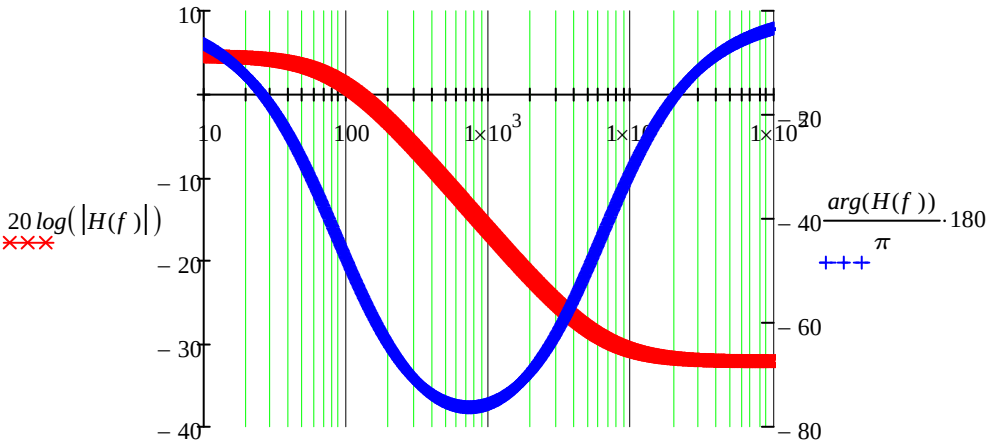


$$R_s := 2\Omega \qquad j := \sqrt{-1} \qquad R_{load} := \frac{V_{out1}^{\,2}}{P_O}$$

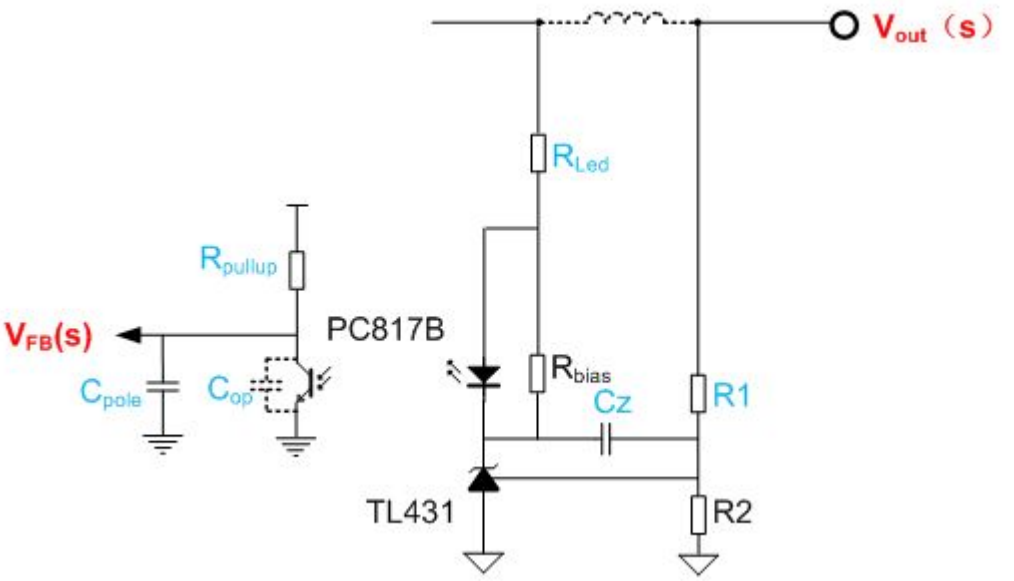
功率级传递函数(Power stage transfer function)：

$$H(f) := \frac{1}{4} \cdot \frac{V_{out1}}{I_{dspeak} \cdot R_s} \cdot \frac{1 + 2 \cdot \pi \cdot f \cdot j \cdot Esr1 \cdot C_{out1}}{1 + 2 \cdot \pi \cdot f \cdot j \cdot \frac{R_{load} \cdot C_{out1}}{2}}$$

According to the Transfer function,we can get the Bode of power stage.



Here, we select Dean Venable Type II as compensation circuit, and the typical circuit in an isolate application with Opto PC817 is:



R1 is the upper divider resistor:

$$R1 := 5k\Omega$$

From the datasheets of PC817 and NCP1015,we can get the inner pullup resister:

$$R_{pullup} := 18k\Omega$$

And the stray opto capacitor, CTR:

$$C_{opto} := 4.3nF$$

$$CTR := 0.4$$

Generally, we dermine the open loop crossover frequency by the output voltage overshoot or undershoot of dynamic load:

Dynamic load: $\Delta I_{out} := 0.8A$

Overshoot Voltage: $\Delta V_{out} := 0.25V$

Select crossover frequency:

$$f_{cross} := \frac{\Delta I_{out}}{2 \cdot \pi \cdot C_{out1} \cdot \Delta V_{out}} = 541.804 \cdot Hz$$

Dermine the mid-band gain:

$$R_{led} := CTR \cdot \frac{R_{pullup}}{10^{-\log\left(\left|H\left(f_{cross}\right)\right|\right)}} = 1.966 \cdot k\Omega$$

Power Stage phase shift:

$$PS := \frac{arg\left(H\left(f_{cross}\right)\right)}{\pi} \cdot 180 = -75.65$$

Set the open loop phase margin:

$$PM := 70$$

Caculate the phase Boost requirement of compensation circuit:

$$Boost := PM - PS - 90 = 55.65$$

Dermine the k Factor:

$$k := tan\left(\frac{Boost}{180 \cdot 2} \cdot \pi + \frac{\pi}{4}\right) = 3.235$$

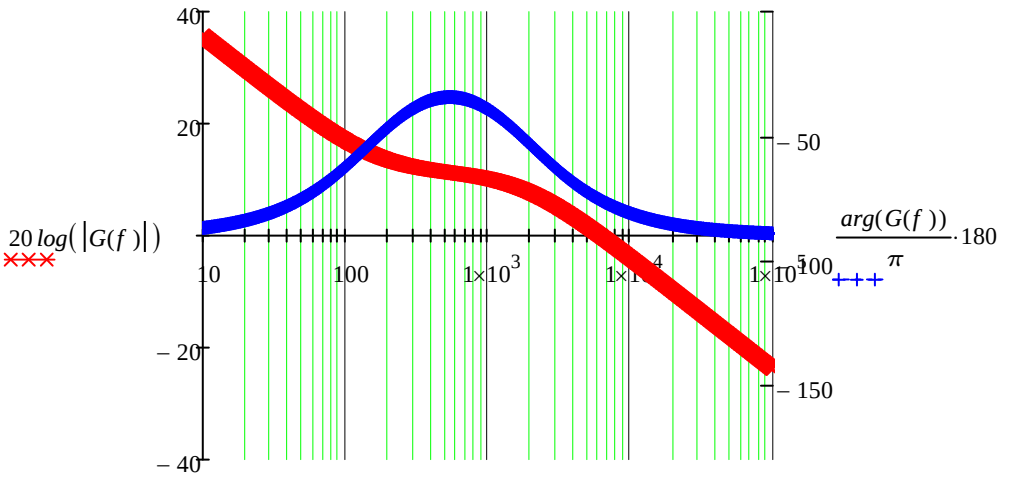
Caculate Cpole and Cz:

$$C_{pole} := \frac{1}{2\cdot\pi\cdot R_{pullup}\cdot k\cdot f_{cross}} - C_{opto} = 0.744\cdot nF$$

$$C_z := \frac{k}{\left(2\cdot\pi\cdot R1\cdot f_{cross}\right)} = 190.085\cdot nF$$

Bode plot of compensation circuit:

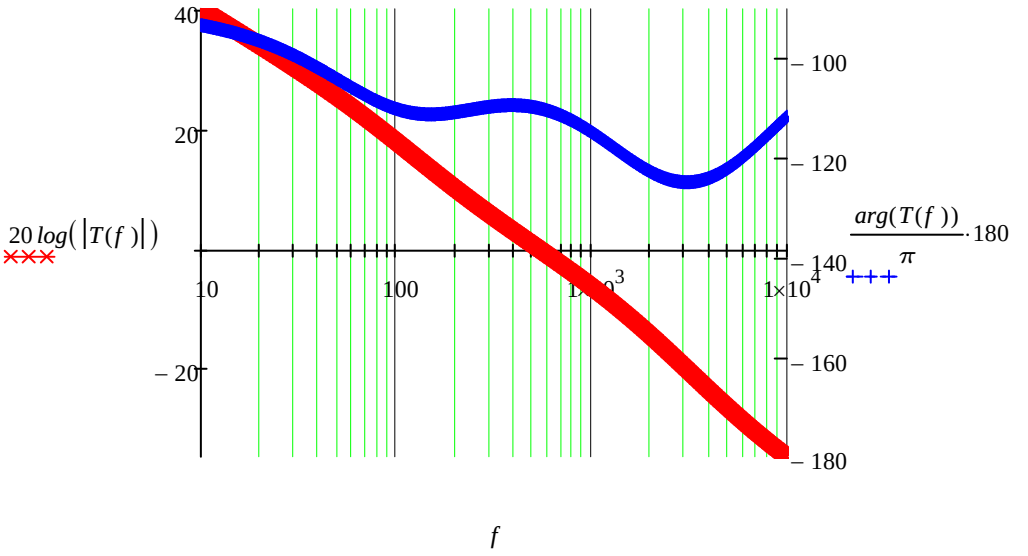
$$G(f) := \frac{R_{pullup}\cdot CTR}{R_{led}}\cdot\frac{1+\frac{1}{2\cdot\pi\cdot f\cdot j\cdot\left(R1\cdot C_z\right)}}{1+2\cdot\pi\cdot f\cdot j\cdot\left[R_{pullup}\cdot\left(C_{pole}+C_{opto}\right)\right]}$$



Combining the power stage and compensation circuit in serial:

$$T(f) := H(f)\cdot G(f)$$

The bode of flyback:



Reference：

[1] Hang-Seok Choi,"Designing Guidelines for Off Line Flyback Converters Using Fairchild Power Switch",Application Note AN4137,www.fairchild.com,2003.

[2] Robert W. Ericson, Dragan Maksimovia, Fundamentals of Power Electronics, second Edition.2003

[3] Christophe Basso,Designing Control Loop for Linear and Swithing Power Supplies,2012.

[4] Dean Venable,"The k Factor: a new mathematical tool for stability analysis and synthesis",Proceedings of Powercon 10, 1983..

[5] 赵修科，《开关电源中的磁性元件》，2003