New Optimization in Photovoltaic Installations with Energy Balance with the Three-Phase Utility

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***Abstract*—The paper propose a new maximum power point tracking (MPPT) system built in the control block, useful for three-phase (4 wires) photovoltaic (PV) generators connected to the utility. The system can be connected directly to the PV panels, avoiding the use of DC/DC converters. The number of sensors is reduced.**

The MPPT algorithm establishes an energy balance between the DC and AC sides through the DC bus voltage control. The three-phase inverter output currents are controlled using a hysteresis-band control. The simulated results show the control loop dynamic response and stability against the most typical perturbations. The PV panel model used in the simulation is described.

I. INTRODUCTION

The exploitation of natural resources is the cause of the photovoltaic market growth. The R&D in this field has been increasing a lot during the last years. Different electronic systems allow for convert the sun radiation in electrical energy. One of the main points in these systems is how to obtain the maximum energy available in the panels. Several MPPT algorithms appear in bibliography ([1,2]).

A typical photovoltaic installation connected to the utility is represented in Fig. 1. The inclusion of a DC/DC converter allows to fix a DC voltage in the inverter input and to implement the MPPT algorithm. The DC/DC converter works like a variable load that adjusts the panel voltage and current to the MPP value. The most typical configuration used is the boost converter because allow to work with a low DC voltage in the solar panel side and increase the output voltage to the requirements of the DC inverter input. The DC/DC converter control voltage reference works with a constant voltage from the input (panel side) which value is the MPP voltage of the solar panel.

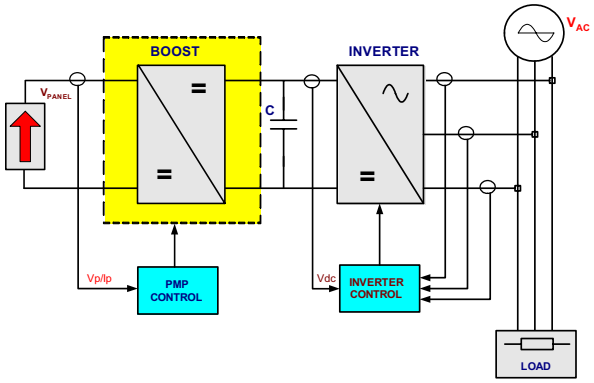

Figure 1. Classic block diagram of a PV installation.

The inverter supplies to the utility the available energy in the DC bus. The output currents are in phase with the corresponding voltages in order to obtain a unity power factor. The control of the DC/DC converter and the inverter are independent and the DC bus is the interface between both converters. The isolation, if it is needed, can be provided with:

- The high-frequency transformer of an isolated DC/DC converter, usually a Full-bridge.
- A low-frequency line transformer connected between the inverter output and the utility. This solution allows for work with a low voltage DC bus and MOSFET transistor instead of the IGBTs used in high voltage inverters.

New MPPT techniques, based in the energy balance between the DC and AC sides, allow for eliminate the DC/DC converter working with a direct connection between the PV panels and the inverter, as appears in Fig. 2. The control is done by a DSP that establish an input voltage equal to the MPP voltage (MPPV) and an output sinusoidal current in phase with the respective phase voltage.

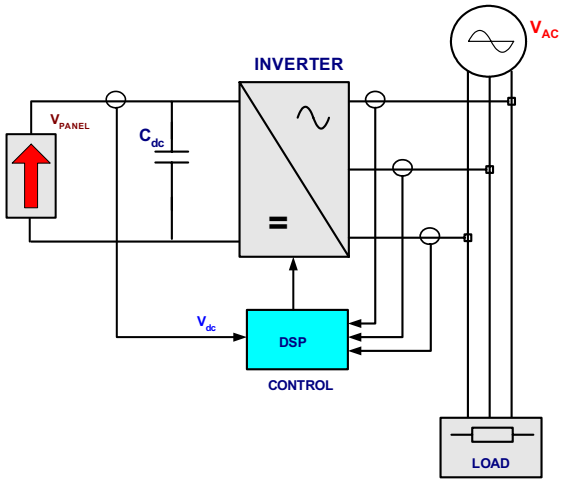

Figure 2. Current generator block diagram of a PV installation

II. MODELING THE SYSTEM

The system under analysis supplies energy to an internal load (solar house in Fig. 3) and the surplus energy is supplied to the utility.

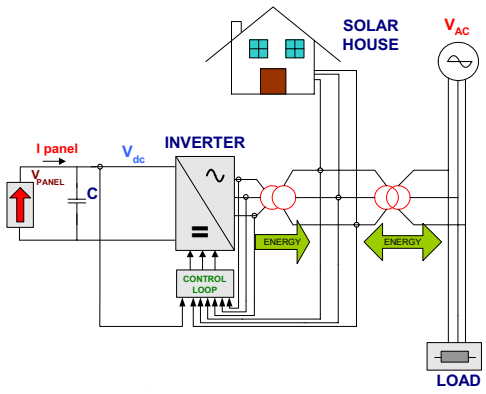

Figure 3. Block diagram of the proposed system.

From the block diagram of Fig. 2, in Fig. 4 is represented the model used for a PV three-phase generator connected to the utility and the load (solar house). The three-phase inverter is built using three half-bridges, as appears in Fig. 4. Ideal switches are used in the simulation. An inductor is connected in the inverter output, working the converter as a controlled current source. The feedback signals are the DC bus voltage, the AC currents in the inverter output and AC load (solar house). The output currents are controlled using a fix hysteresis band.

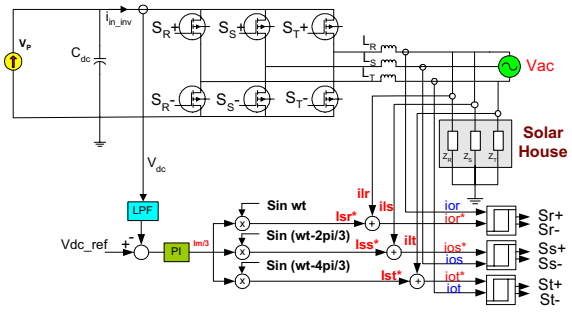

Figure 4. Block diagram of the proposed system.

A. *PV panel model*

The typical equivalent circuit of a PV panel is represented in Fig. 5. The behavior of a solar cell is usually modeled like (1) [3-4].

$$I_P = I_{sc} - I_o \cdot \left(e^{\left[\frac{q}{AKT}(V_p + I_P R_s)\right]} - 1 \right) \tag{1}$$

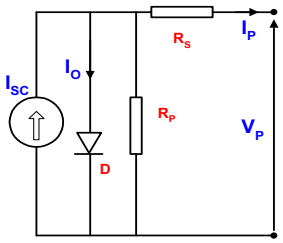

Figure 5. PV panel equivalent circuit

Where:

- I_P is the generated cell current
- I_{SC} is the short circuit a darkness cell current
- I_o is the reverse saturation current (leakage current)
- V_p is the panel voltage.
- R_S is the output serial resistance of the solar cell and R_p is parallel resistance.
- K is the Boltzman's constant.
- T is the temperature (Kelvin)
- Q is the electron charge.
- A is the ideally factor for a PN junction.

The output serial resistance has low value, around 100mΩ, so the voltage drop is low enough to avoid it ($I_P \cdot R_s \to 0$). With this approximation the current produced by a cell is:

$$I_P = I_{sc} - I_o \cdot \left(e^{\left[\frac{q}{AKT} V_p\right]} - 1 \right) \tag{2}$$

Due to $I_o << I_{SC}$, the current produced by a cell is:

$$I_P = I_{sc} - I_o \cdot e^{\left[\frac{q}{AKT} V_p\right]} \tag{3}$$

The term that is multiplying the panel voltage has voltage units and is constant for a specified panel and a working temperature. For that conditions $\frac{AKT}{q} = V_o = const.$, then

$$I_P = I_{sc} - I_o \cdot e^{\left[\frac{V_p}{V_o}\right]} \tag{4}$$

For a PV cell array (4) represent the current and voltage behavior of the panel, and can be used for the PV panel model if the terms V_o and I_o are known. The short-circuit current (I_{SC}), the open-circuit voltage (V_{OC}) and the peak power ($P_{pk\ panel}$) of the panel are the main data used to do the installation design.

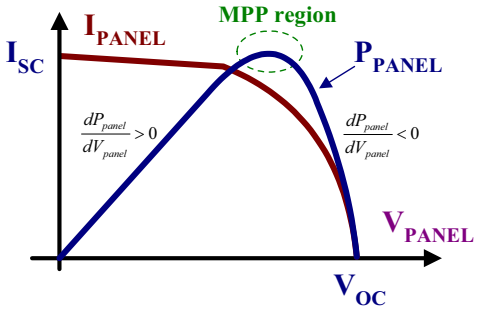

Figure 6. PV panel characteristics.

When the panel voltage is equal to the open-circuit voltage (V_{OC}), the current I_S is null. At this working point:

$$I_P = 0 = I_{sc} - I_o \cdot e^{\left[\frac{V_{OC}}{V_o}\right]}$$
$$I_o = \frac{I_{sc}}{e^{\left[\frac{V_{OC}}{V_o}\right]}} \tag{5}$$

From experimental results [5], in the MPP region, for a voltage change of 1V around the best MPP, only produces

a minimum power change, smaller than 5%. The MPP region is situated around the following values:

- $V_{MPP} = MPPV \approx 0.8 \cdot V_{OC}$.
- $I_{MPP} = MPPI \approx 0.9 \cdot I_{SC}$.

Replacing the MPP voltage and current in (4):

$$I_{P\_MPP} = I_{sc} - I_o \cdot e^{\left[\frac{V_{MPP}}{V_o}\right]}$$
$$0.9 \cdot I_{sc} = I_{sc} - I_o \cdot e^{\left[\frac{0.8 \cdot V_{OC}}{V_o}\right]} \quad (6)$$

The value of V_o is:

$$V_o = \frac{0.2 \cdot V_{OC}}{\ln(10)} \quad (7)$$

Replacing this expression in (5):

$$I_o = \frac{I_{sc}}{e^{\left[\frac{V_{OC}}{\frac{0.2 \cdot V_{OC}}{\ln 10}}\right]}} = \frac{I_{sc}}{e^{\left[\frac{\ln 10}{0.2}\right]}} \quad (8)$$

With the values of these constants depending on the short-circuit current (I_{SC}) and the open-circuit voltage (V_{OC}), the PV panel is modeled in Matlab/Simulink (Fig. 7). The model represented in Fig 7. implement (4), where I_{SC_ref} is the I_{SC} of the selected panel, CCS* blocks represent Current-Controlled Sources and Fcn block is:

$$Fcn = I_o \cdot e^{\left[\frac{V_p}{V_o}\right]} \quad (9)$$

The output serial resistance is not included in the model due to its low value.

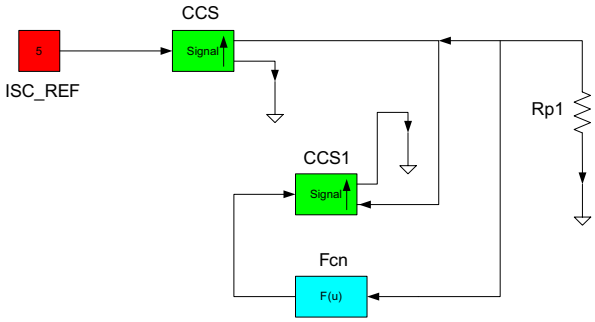

Figure 7. Solar panel model in Simulink

B. Inverter model

The inverter model take care that the inverter is controlled to find unity power factor. The inverter output reference currents ($i_{out\_ref\_*}$) are obtained for each phase with the block diagram of Fig. 4, for the three phases, and Fig. 8 for one phase. The maximum surplus current that can be generated (I_m) is obtained after the PI regulator [6], the error signal between the DC bus voltage and its reference (MPP voltage). The current I_m is multiplied by a unity sinus and with the corresponding phase delay depending on the phase. The three-phase currents supplied to the utility represent a constant flux of energy from the PV panel to the load (solar house and the grid). The three phase reference currents are used to implement the output current control. A hysteresis band controller with a fix band is used in the simulation.

The relation energy balance between the DC and AC sides.

$$P_{DC} = MPPV \cdot I_{DC} \approx P_{AC} = 3 \cdot V_L \cdot I_{out\_inv} \quad (10)$$

V_L is the rms value of the line voltage (average value of the three phases) and I_{out_inv} is the rms value of the generated line current (inverter output current).

The MPPV voltage in the DC bus is equal to its reference value (V_{dc_ref}). Due to the current controller, the I_{out_inv}, is equal to the I_{out_ref}. The DC current is equal to:

$$I_{DC} = \frac{3}{\sqrt{2}} \frac{V_L}{V_{dc\_ref}} I^*_{out\_peak\_ref} \quad (11)$$

From (11) Kc, can be obtained like in (12) which represent the inverter model.

$$Kc = \frac{3}{\sqrt{2}} \frac{V_L}{V_{dc\_ref}} \quad (12)$$

Due to the switching frequency is high (>15kHz) and the output inductor is small, the equation for the output current inverter is:

$$i_{out\_inv} = K_c \cdot i_{out\_ref*} \quad (13)$$

The inverter output phase current is (Fig. 4):

$$i_{out\_inv} = i_{Load\_House} + i_S \quad (14)$$

Where i_S is the surplus sinusoidal current. The i_{Load_House} can be non linear.

This equation is represented at the end of the control block diagram in Fig. 8.

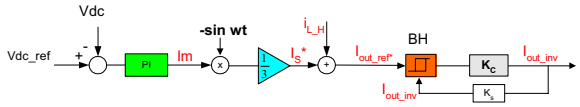

Figure 8. *Inverter model and control loop for a single phase.*

C. DC bus capacitance

In an ideal three-phase generator the energy flow is constant if the currents are in phase with the voltages and each phase is delayed 120° from the others. With a balanced set of voltages in the utility and fundamental currents ($I_{out\_inv\_1}$) in the output of the inverter, the instantaneous energy (e(t)) obtained (15).

$$e(t) = \int p(t)dt = \int (v_R \cdot i_R + v_S \cdot i_S + v_T \cdot i_T)dt$$
$$e(t) = 3 \cdot V_L \cdot I_{out\_inv\_1} \cdot t \quad (15)$$

The energy that flows from the PV panel is also constant, so there is an energy balance between the DC and AC side (16). Due to that, the ripple in the DC bus capacitance is null [7], appearing only a small ripple due to the switching of the power semiconductors.

$$E_{DC} = MPPV \cdot I_P \cdot T$$
$$E_{AC} = 3 \cdot V_L \cdot I_{out\_inv\_1} \cdot T \quad (16)$$
$$if \quad E_{DC} \approx E_{AC} \Rightarrow \Delta V_{bus\,DC} \rightarrow 0$$

The design of the DC bus capacitance is done using a capacitor ten times smaller than the needed in a single-phase case with the same output phase current. The instantaneous energy in single-phase systems is:

$$e(t) = \int [V_L \cdot \sin(\omega t)] \cdot [I_{out\_inv\_1} \cdot \sin(\omega t)] dt$$
$$e(t) = \int V_L \cdot I_{out\_inv\_1} \cdot (1 - \cos 2\omega t) dt \quad (17)$$
$$e(t) = V_L \cdot I_{out\_inv\_1} \cdot t - \frac{V_L \cdot I_{out\_inv} \cdot \sin 2\omega t}{2\omega}$$

The first term is constant and the second has a sinus variation with a frequency twice of the utility frequency. This second term produce a voltage ripple in the capacitor. The variation of energy, peak to peak, due to this second term is:

$$\Delta E_{pk-pk} = 2 \frac{V_L \cdot I_{out\_inv\_1}}{2\omega} \quad (18)$$

If the voltage in the capacitor varies between a maximum value ($V_{dc\_max} = V_{dc} + \Delta V_{dc}$) and a minimum value ($V_{dc\_min} = V_{dc} - \Delta V_{dc}$), the variation of energy in the capacitor is:

$$\Delta E_{pk-pk} = \frac{1}{2} C_{dc} \left[(V_{dc\_\max})^2 - (V_{dc\_\min})^2 \right] \quad (19)$$
$$\Delta E_{pk-pk} = 2 \cdot C_{dc} \cdot V_{dc} \cdot \Delta V_{dc}$$

Equaling (18) and (19), the capacitor for the single-phase case is designed as:

$$2 \cdot C_{dc} \cdot V_{dc} \cdot \Delta V_{dc} = \frac{V_L \cdot I_{out\_inv\_1}}{\omega}$$
$$C_{dc} = \frac{V_L \cdot I_{out\_inv\_1}}{2 \cdot V_{dc} \cdot \Delta V_{dc} \cdot \omega} \quad (20)$$

So, for the three-phase systems the value of the capacitance is:

$$C_{3p\_dc} = \frac{1}{10} \frac{V_L \cdot I_{out\_inv\_1}}{2 \cdot V_{dc} \cdot \Delta V_{dc} \cdot \omega} \quad (21)$$

D. PI regulator design

The DC voltage is controlled by means of the sinusoidal output currents. The DC voltage control block diagram is in Fig. 9. The relation between the capacitor voltage and current, using the panel current (I_P) and the inverter input current (i_{in_inv}), is:

$$\frac{dV_{dc}}{dt} = \frac{1}{C_{dc}} \left(I_P - i_{in\_inv} \right) \quad (22)$$

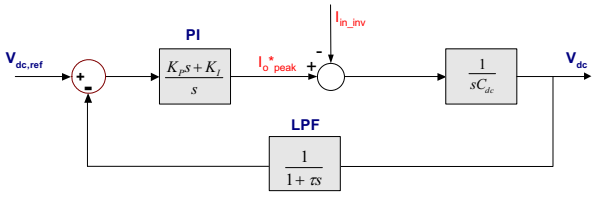

Figure 9. DC voltage control block diagram.

The DC bus voltage control loop (MPP control) response time depends on the delay and the PI regulator gain. If a change in the DC voltage reference is applied, the system shows a delay due to the power stage, the low pass filter (LPF) and mainly by the PI regulator. Analyzing the close loop transfer function [2] and equaling to zero, we obtain

$$s^3 + \frac{1}{\tau} s^2 + \frac{K_p \cdot K_c}{\tau \cdot C_{dc}} s + \frac{K_i \cdot K_c}{\tau \cdot C_{dc}} = 0 \quad (23)$$

where:

- K_p is the proportional constant of the PI regulator.
- K_i is the integral constant of the PI regulator.
- K_c is the constant that models the inverter block.

If the LPF has a delay time near to zero ($\tau \to 0$), the equation is simplified [2], Kp and Ki are given as follows.

$$K_p = \frac{4C_{dc}}{\tau_{PI} \cdot K_c} \qquad K_i = \frac{K_p}{\tau_{PI}} \quad (24)$$

The criterion relation of the delay time of the systems (τ) and the PI delay is obtained.

$$\tau_{PI} > 5\tau \quad (25)$$

With this relation is possible to meet at the same time a good stability, a small oscillation and a null position error. The control system response can be improved with an increase in the PI regulator gain (K_P), with the limits established by (25).

III. SYSTEM CONFIGURATION

During the simulations we are using a model that correspond to the PV panels array with V_{OC}=500V and I_{SC}=5A is used. Using (7) and (8) the values of I_O=50μA and V_o=43.43V are obtained. With these values the PV panel model can be implemented.

The DC bus reference voltage is V_{DC_ref}=399V (MPPV of the array of panels). With an rms line voltage V_L=125V, (12) give K_c=0.664. The input power at MPP is around 1800W, and the maximum DC bus ripple voltage is limited to 10V, so the DC bus capacitance from (21) is 220μF. For the LPF the delay time is τ=3ms (corner frequency of 50Hz), so the PI regulator minimum delay time is 15ms. The selected τ_{PI} is equal to 50ms, so from (24) K_p=0.354 and K_i=14.16 in the PI regulator. The output inductance is 7mH and the equivalent solar house-load is 80Ω, per phase.

IV. SYSTEM SIMULATION

Some simulations with Matlab(6.5)/Simulink have been done with the values obtained in the previous section. The control section of the three-phase inverter connected to the utility is showed in next figures.

The *Solar Panel* block corresponds to the sub circuit represented in Fig (11). The output DC voltage from the panel is the power input of the *Inverter* block. The inverter is supplying energy to the house loads and to the utility (14), represented both in the three blocks at the right side of Fig 3. Each phase have their own *Control loop* block. The phase voltage is used as a reference signal (unity power factor in the output), the two currents and the

filtered DC voltage are used to obtain the references currents control the inverter switches.

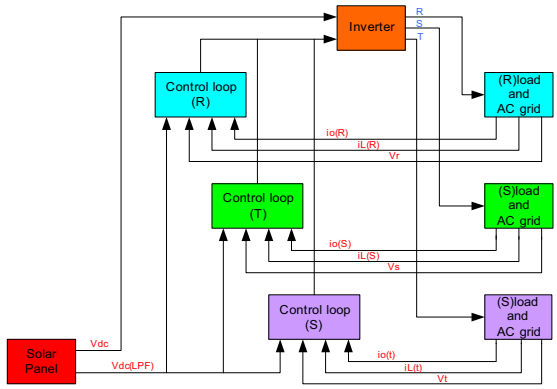

Figure 10. General block diagram.

The *Solar Panel* subsystem is represented in Fig 11 and is equivalent to the analyzed in section II.A.

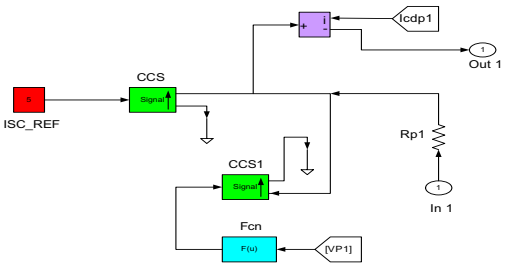

Figure 11. Solar panel subsystem.

The *Control loop* block for phase S is represented in Fig 12. For phases R and T are similar. The inputs in1 to in4 are the feedback signals (Fig 10):

- In1 is the output current in the phase
- In2 correspond to the house-load current.
- In3 is assigned to the instantaneous phase voltage. The PLL block allows obtaining a unity sinusoidal signal synchronized with the voltage utility.
- In4 is the filtered DC bus voltage (V_{DC_LPF}).

The outputs of the different blocks are:

- Out1: output current of the inverter.
- Out2: output load of the inverter.
- Out3: utility voltage.

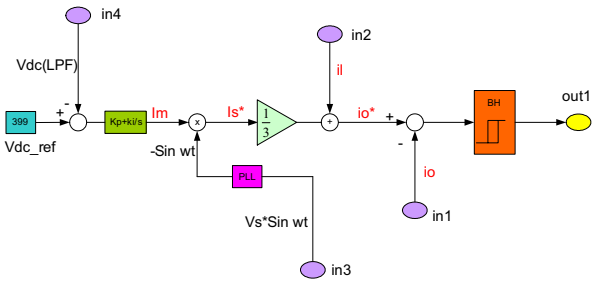

Figure 12. Control loop block diagram per phase

The current control is implemented using a hysteresis band controller (BH block). This technique simplifies the control and is extremely robust [8]

The phase load and the utility (block *(*)load and AC grid* in Fig. 10) are modeled in Fig. 13. Part of the inverter output current flows through the house-load (RL(*) in Fig. 13 and the remainder is supplied to the utility.

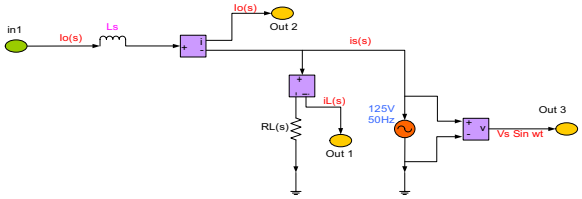

Figure 13. (*)load and AC grid block diagram

The simulation results are presented in the following sections. The simulation needs 50ms to establish the signals in the correct values. This time is imposed by the LPF used in the DC bus voltage measurement.

A. DC Power response.

The DC bus reference voltage is fixed to 399V. The DC power is constant (fig. 14) and the AC currents are in phase with the respective voltages (fig. 15).

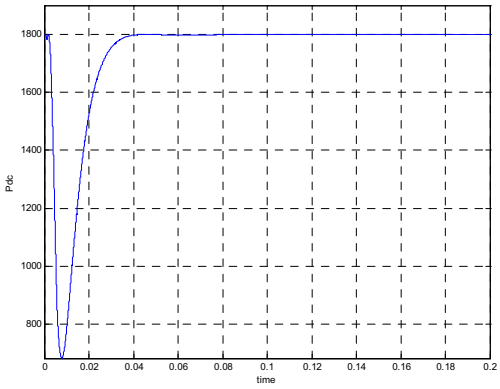

Figure 14. Instantaneous DC bus power.

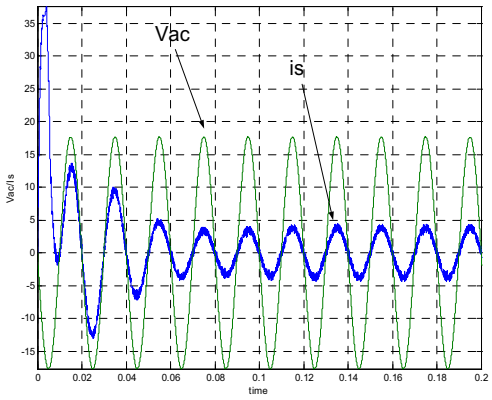

Figure 15. Phase voltage (v_{ac}) and surplus current (i_{SP}) in phase R.

B. Response to a change in the reference V_{dc_ref}.

The DC voltage reference is changed from 399V (nominal value) to 350V in t=0.25s.

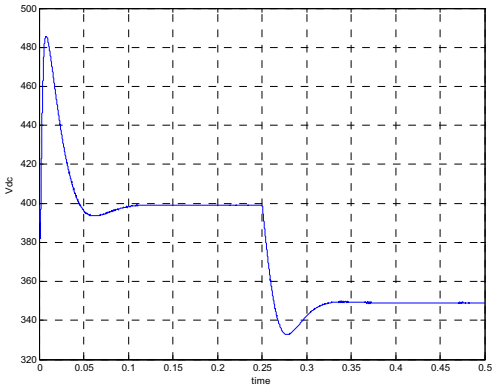

Figure 16. DC bus voltage

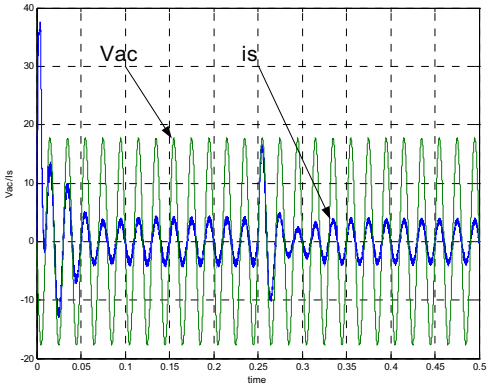

Figure 17. Phase voltage (v_{ac}) and surplus current (i_s) in phase R.

C. *Response to a radiation change.*

The variation in the radiation is done changing the MPPI from 4.5 A to 3.5 A in t=0.25s.

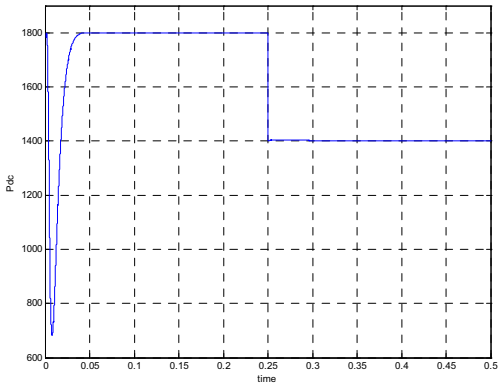

Figure 18. Instantaneous DC bus power.

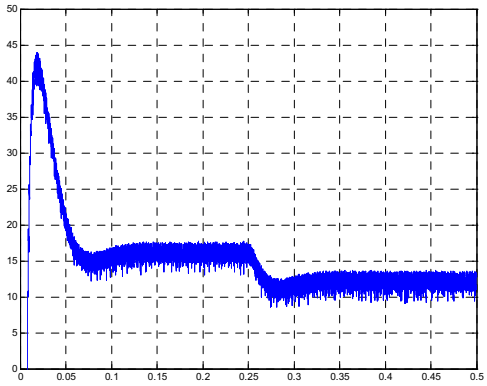

Figure 19. Three-phase instantaneous power.

D. *Response to a load change.*

The phase load changes from 80Ω to 34Ω in t=0.25s. The instantaneous power in the DC bus is nearly constant during the transition (fig. 20). After the transition the load current increases so the surplus current decreases, maintaining energy balance between the DC and AC side (fig. 21).

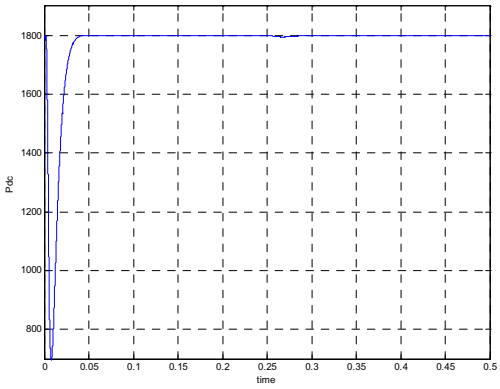

Figure 20. Instantaneous DC bus power.

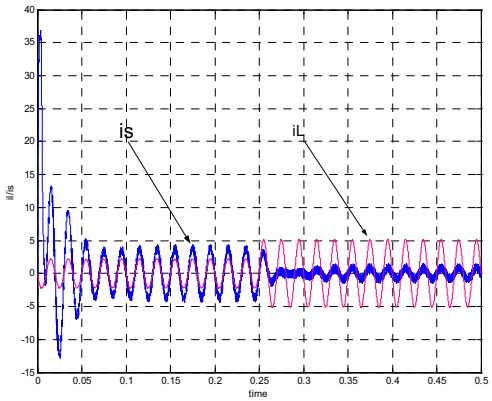

Figure 21. Surplus current (i_s) and load current (i_L).

E. Response to an utility change.

The phase voltage changes from 125V to 110V (rms values) in t=0.25s. The over voltage in the DC bus is smaller than 2% (fig. 22). Due to the energy balance between the DC and AC side, after the transition the currents increases (fig. 23).

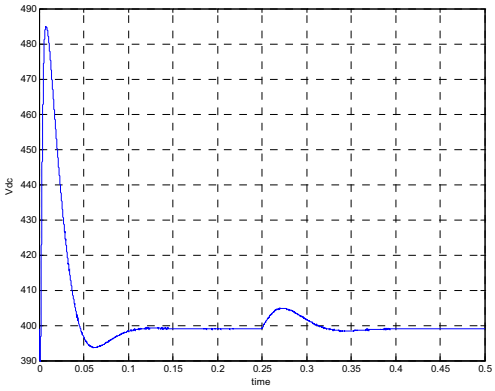

Figure 22. DC bus voltage

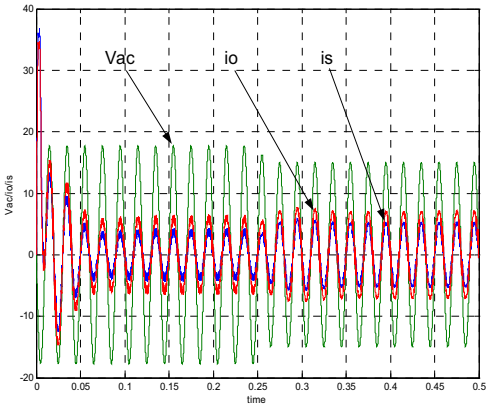

Figure 23. Phase voltage (v_{ac}), inverter output current (i_o) and surplus current (i_s) in phase R.

V. CONCLUSIONS

The proposed MPP controls introduce a simplification in the power stage and in the control section. The energy balance control between the DC and AC sides allows for eliminating the DC/DC converter, with a weight and cost reduction. The efficiency is improved if is compared with classic methods. The simplifications can be done if the voltage from the PV panel is higher than the maximum voltage in the grid. In this case, the voltage difference between the DC bus and the utility allow to perform a good current tracking.

The hysteresis current controller used in the simulation shows a good transient response and its implementations are easier than other current controller used in similar applications.

The results obtained with Matlab/Simulink for a low-power model are good, so in next weeks the power rating will be increased to 6kW. At the same time, a three-phase inverter is in development in our research laboratories and experimental results will be obtained.

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